**Integrated Design and Simulation Environment for a Space Qualified Onboard Computer**

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1. **Abstract**

This paper presents a simulation facility used for the verification and validation of Onboard Computers. The simulation facility was utilized to test a recently developed Onboard Computer. Particularly, the presented platform aims at the verification and validation of embedded systems rather than control algorithms [1] [2]. The facility consists of a Hardware-in-the-Loop Simulation platform, which feeds the target Onboard Computer with signals coming from various distributed spacecraft components. Such spacecraft components can be either hardware components interfaced with the platform or other systems emulated by the computer running the simulation.

The architecture of the Integrated Design and Simulation Environment (IDSE) is shown in figure 1. Starting from the right end of the figure, there is the programming computer. The programming computer is connected to the Onboard Computer, also known as Spacecraft Management Unit (SMU), through dedicated Ground Support Equipment (GSE). The SMU is in this case the main test unit. The simulation server is connected to the SMU in three different ways to cover all the possibilities of interacting with the test unit, i.e., CAN bus port, SpaceWire port, and power inlet.

In parallel, the simulation includes the models of various subsystems, such as sun sensors and reaction wheels. The simulation computer can interface with a camera that is utilized during the simulation as a navigation camera (NavCam). Additionally, the simulation computer interfaces wirelessly with a training satellite, called EyasSat. Such a satellite is a simplified version of a real satellite, and it includes the most common subsystems present in actual orbiting satellites, such as an attitude determination and control system [3]. Furthermore, the dynamics of such training satellite can be emulated in orbital conditions, since it is mounted on a floating-base, five-degree-of-freedom air-bearing stand. In conclusion, the current setup allows for testing the SMU's functionality by interfacing modelled and actual hardware in an emulated space environment.

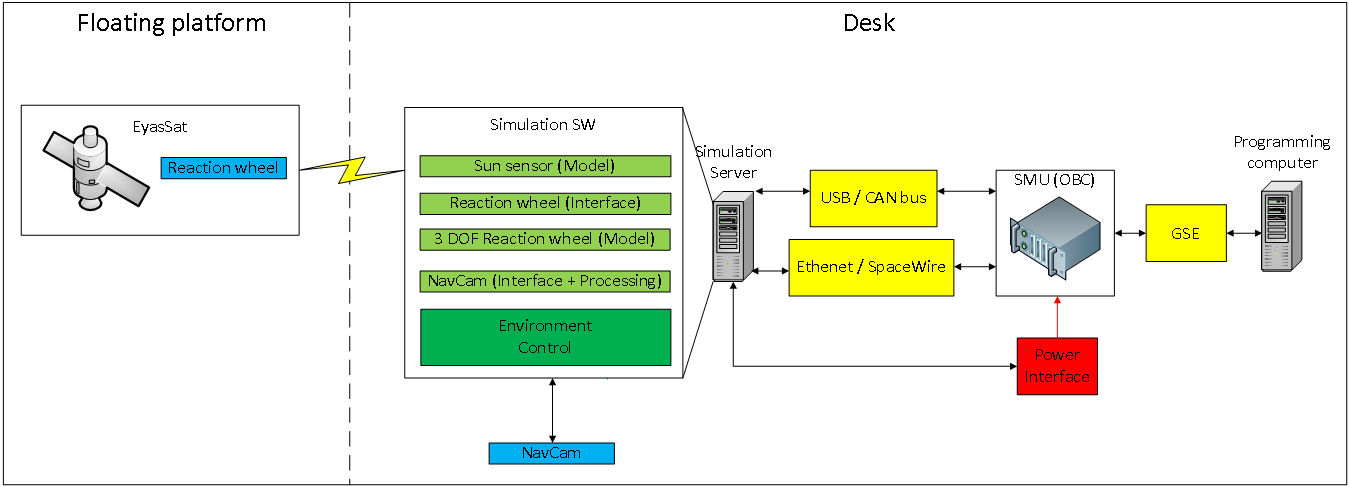


Figure 1: Architecture of the IDSE.

1. **References**

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