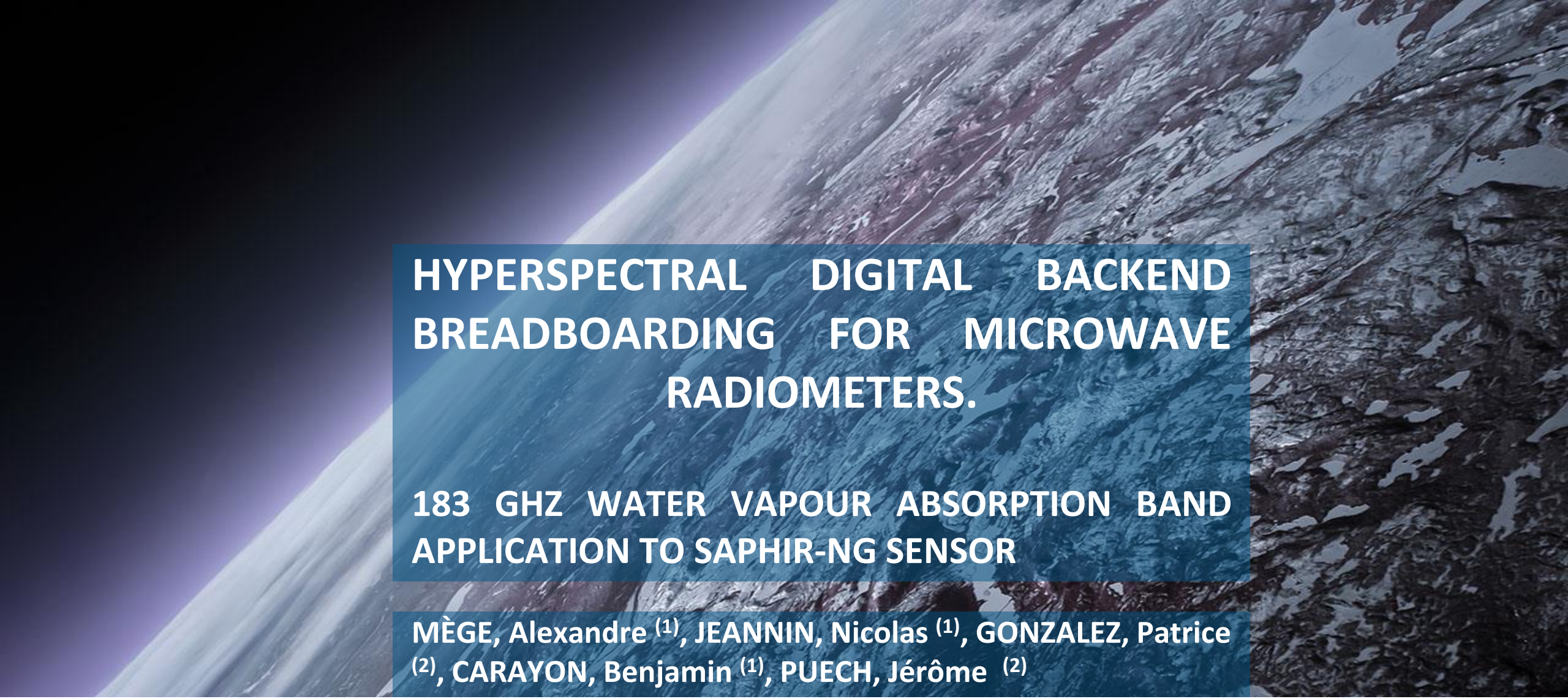

HYPERSPECTRAL DIGITAL BACKEND BREADBOARDING FOR MICROWAVE RADIOMETERS.

183 GHZ WATER VAPOUR ABSORPTION BAND APPLICATION TO SAPHIR-NG SENSOR

MÈGE, Alexandre [(1)], JEANNIN, Nicolas [(1)], GONZALEZ, Patrice [(2)], CARAYON, Benjamin [(1)], PUECH, Jérôme [(2)]

(1) AIRBUS DEFENCE AND SPACE
(2) CNES - Service Instrumentation Radar et Performances

OBDP 2021, 2021-06-14

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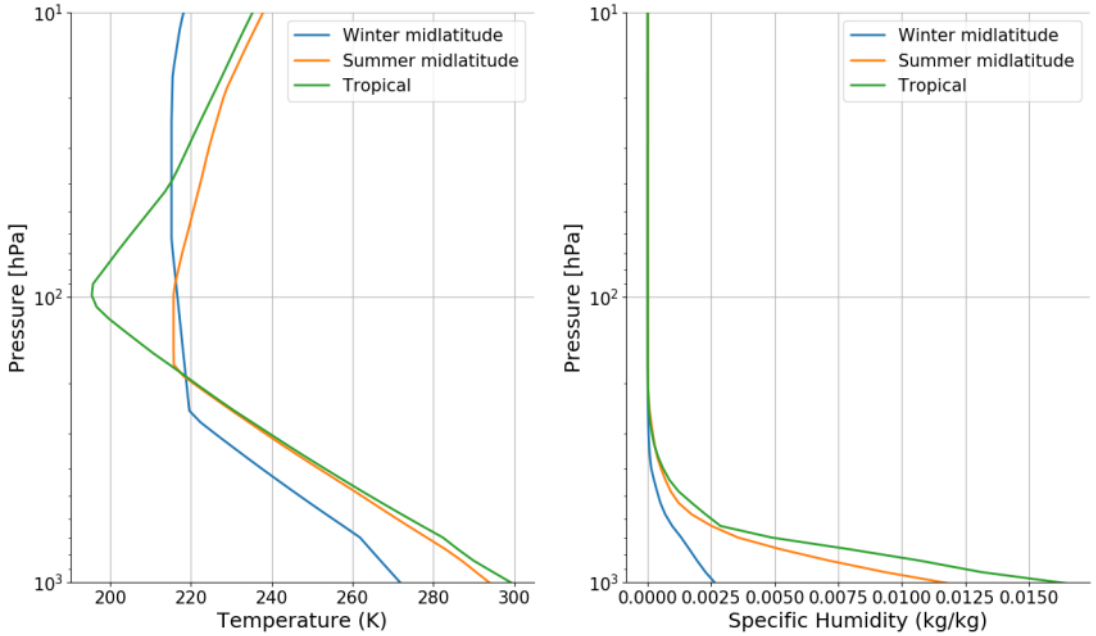
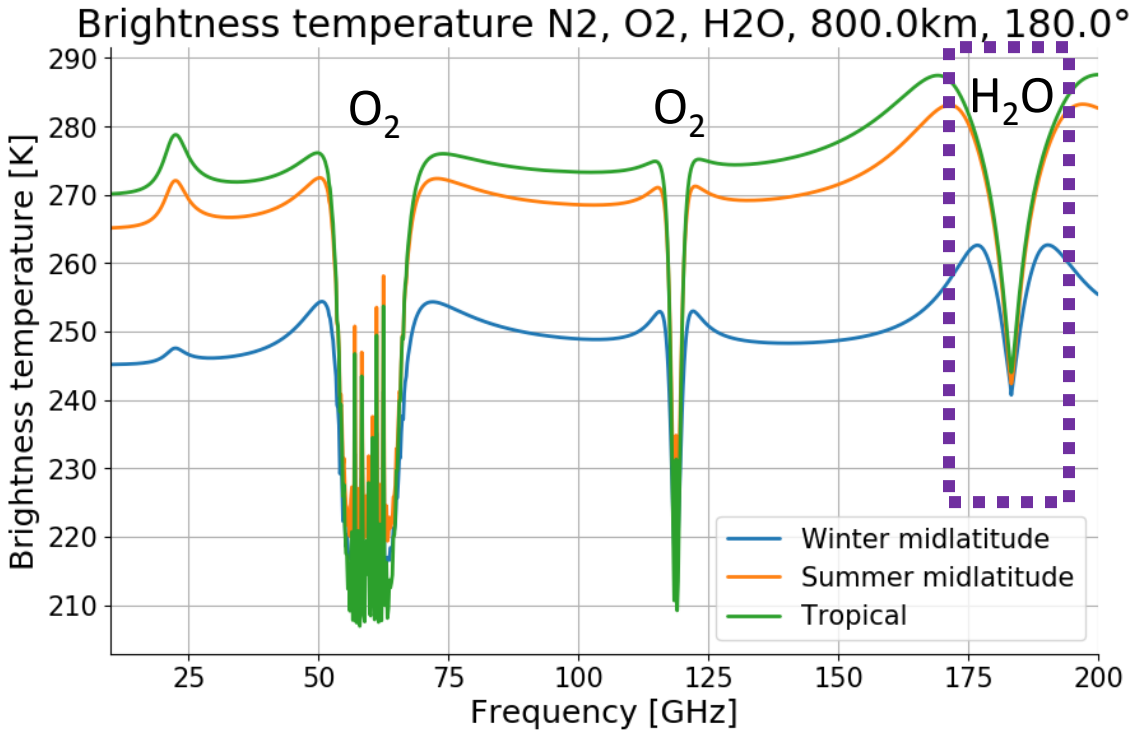
Microwave atmospheric sounding principle (1/2)





Brightness temperature over 10-200 GHz computed using the software ARTS

Brightness Temperature (= Spectral power density) depends on

- Frequency
- Atmospheric state
  - Specific humidity vs altitude
  - Temperature vs altitude

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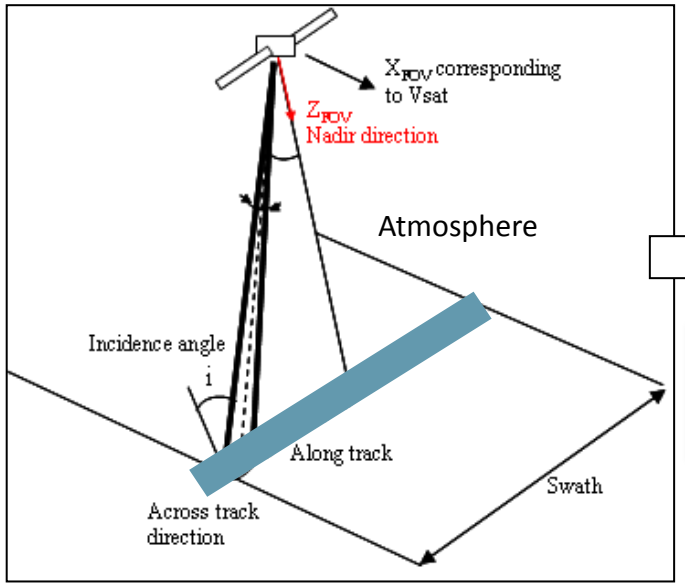
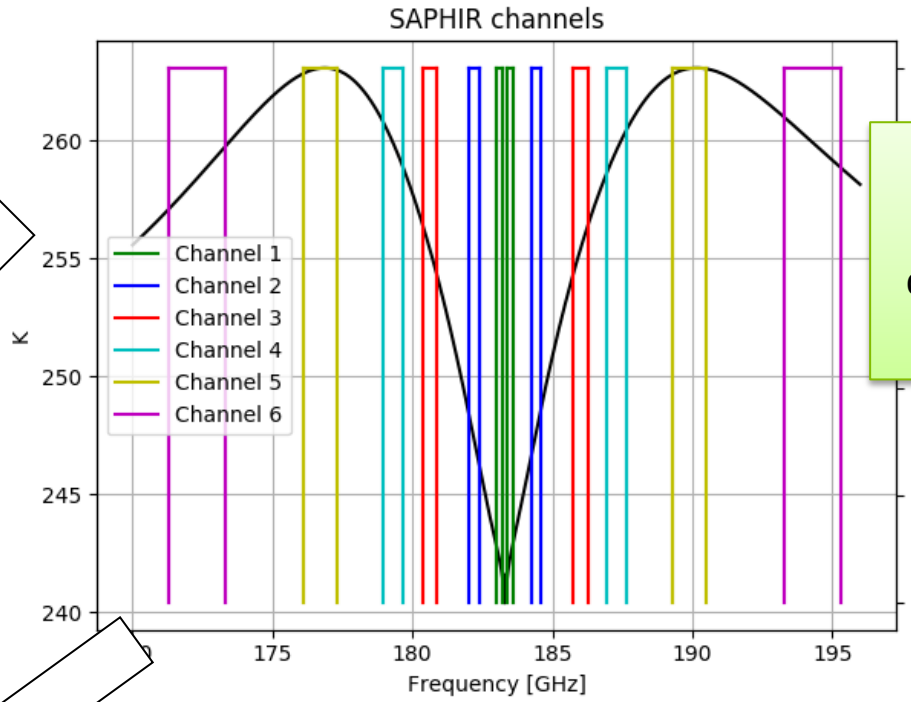
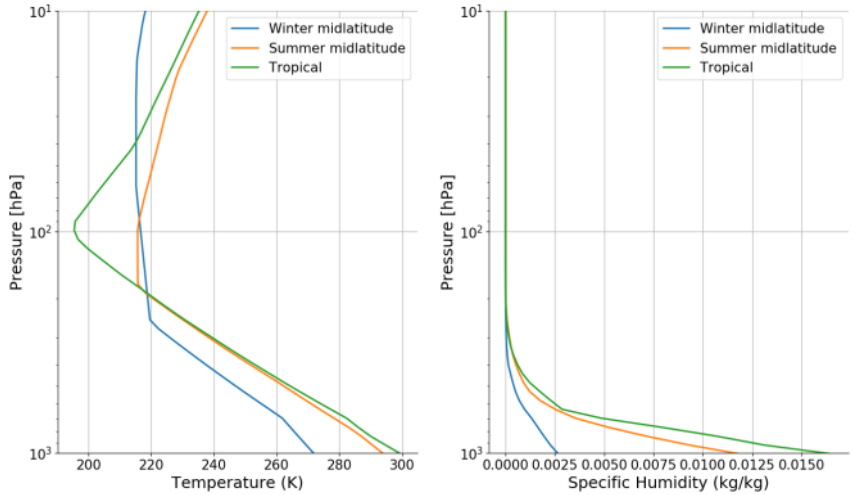
Microwave atmospheric sounding principle (2/2)



Passive microwave sounder



Measure noise spectral power density in multiple channels



Invert the measurement to recover the atmospheric profile

Interest for more channels :

- Increases the quality of the inverted profiles by having mode information

But requires digital filtering

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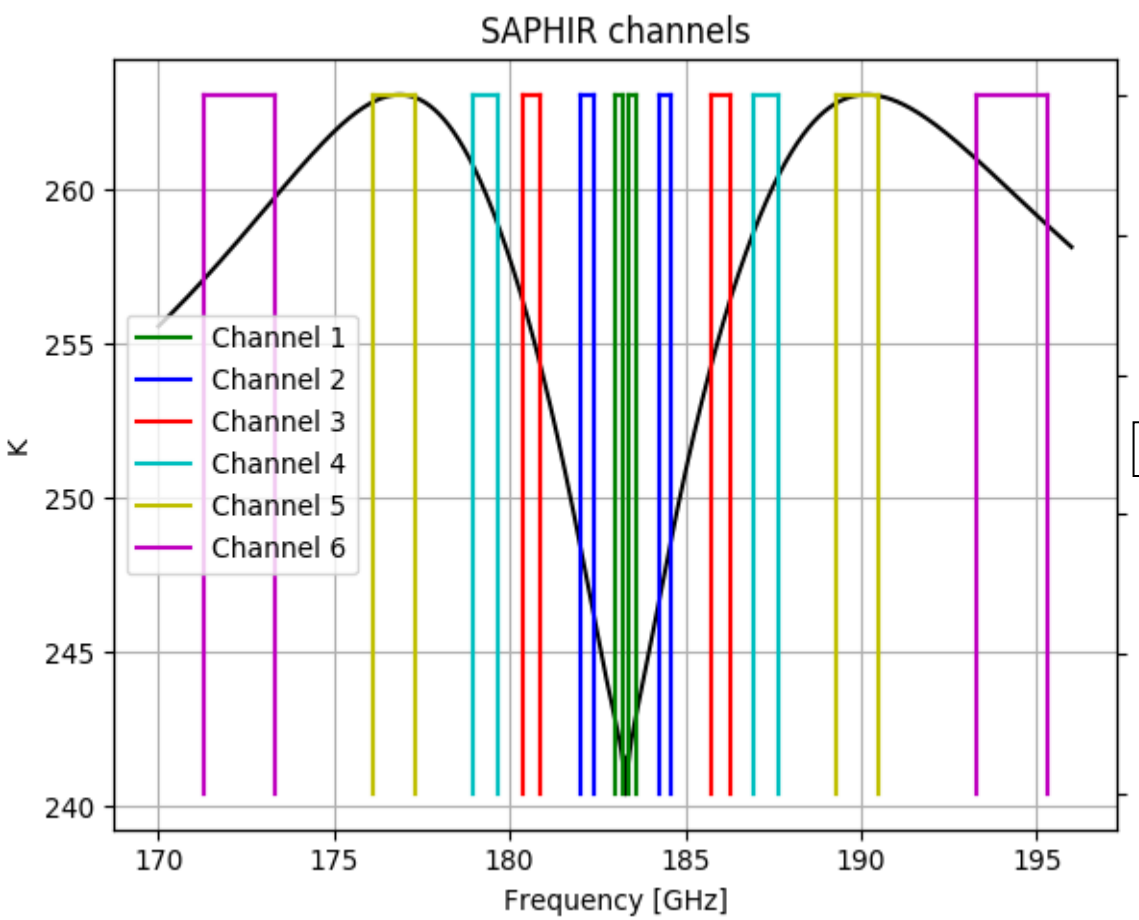
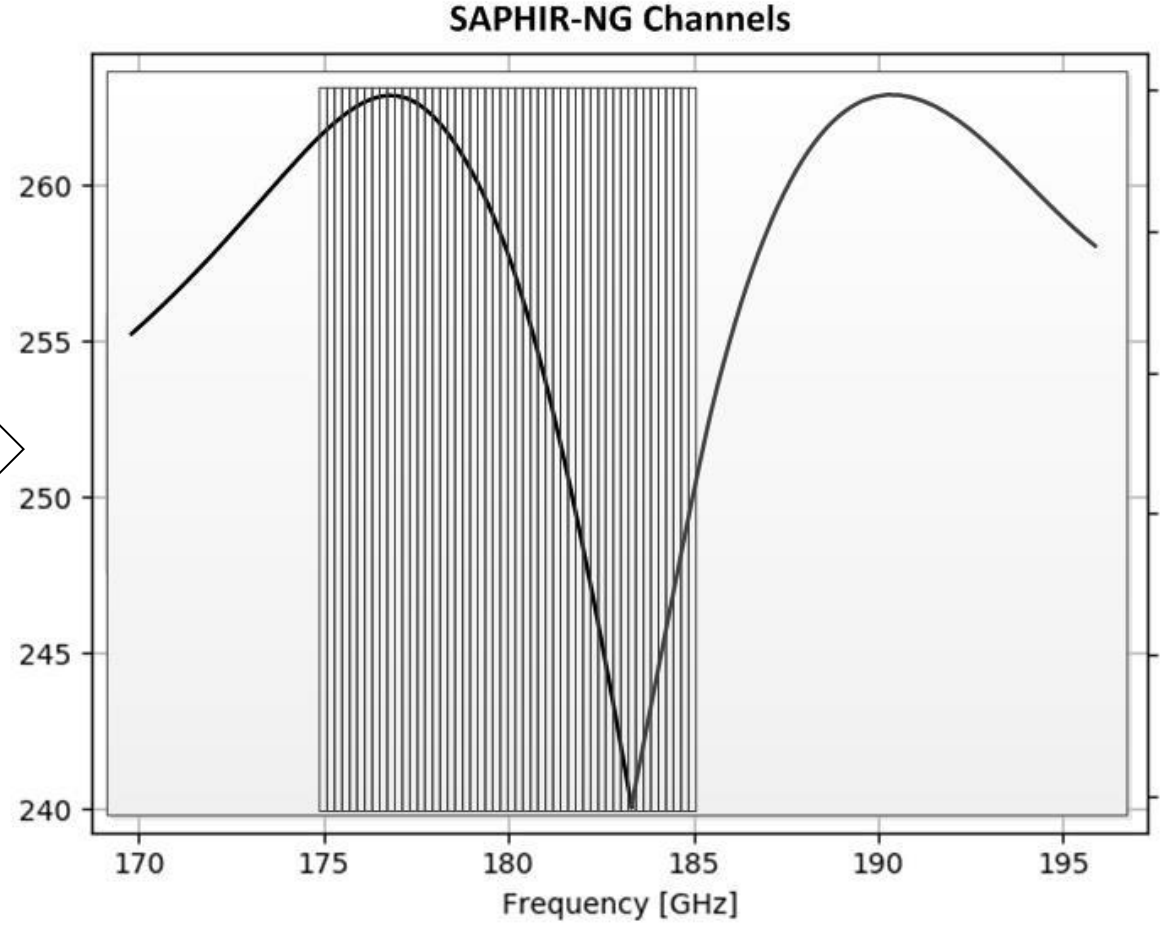
From SAPHIR to SAPHIR-NG





6 Channels (Single Side Band) : 0,2 to 2 GHz BW

10 GHz BW, >100 channels

Digital channelisation

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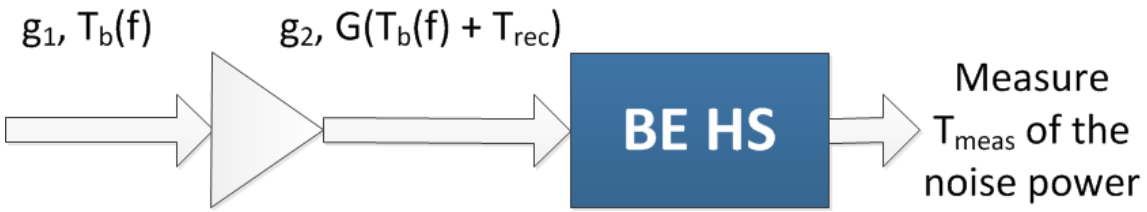
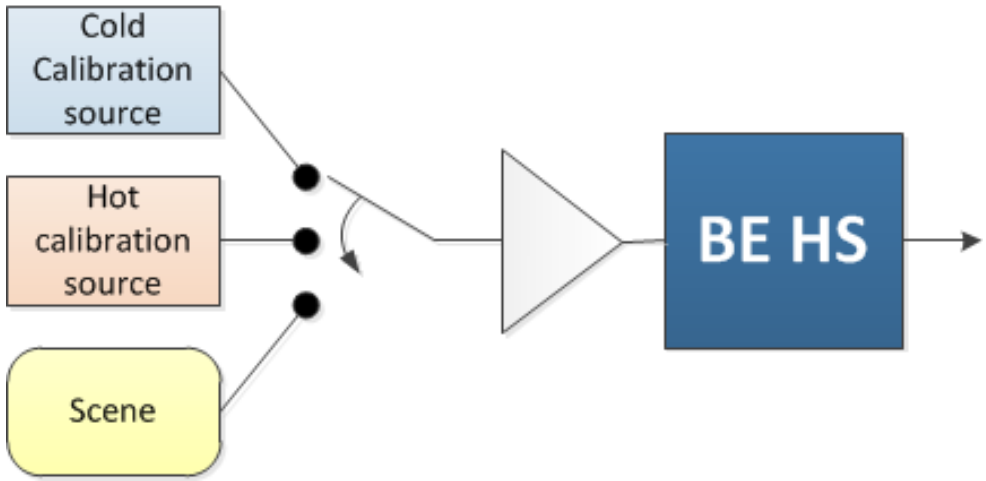
Performance goals

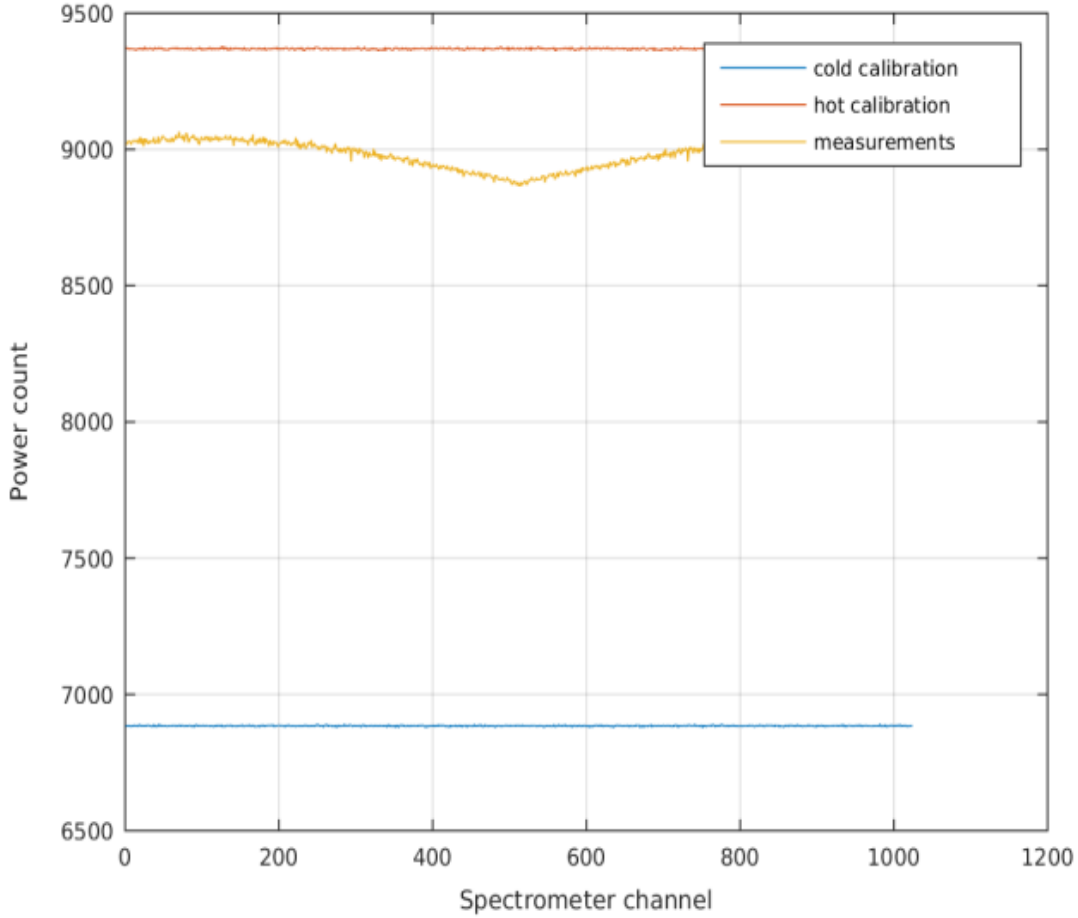
- Bandwidth B_T > 10 GHz
- Max radiometric bias increase **0.1K**
- Power consumption <10 W
- Frequency selectivity <-40 dB (at TBC MHz from filter center)

Acquisition chain model and calibration

Need to calibrate gain and noise temperature of the chain







Calibration uses a cold source (cold sky) and a hot source (metrology hot source)

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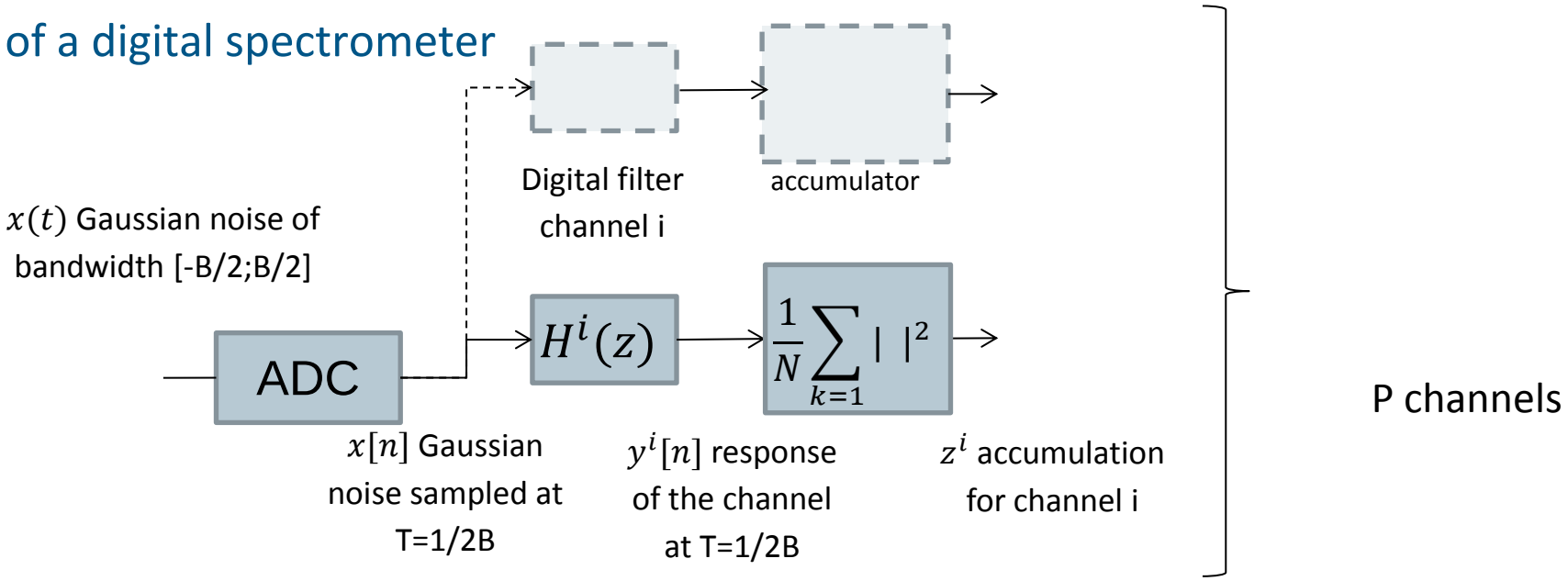
Processing and algorithm

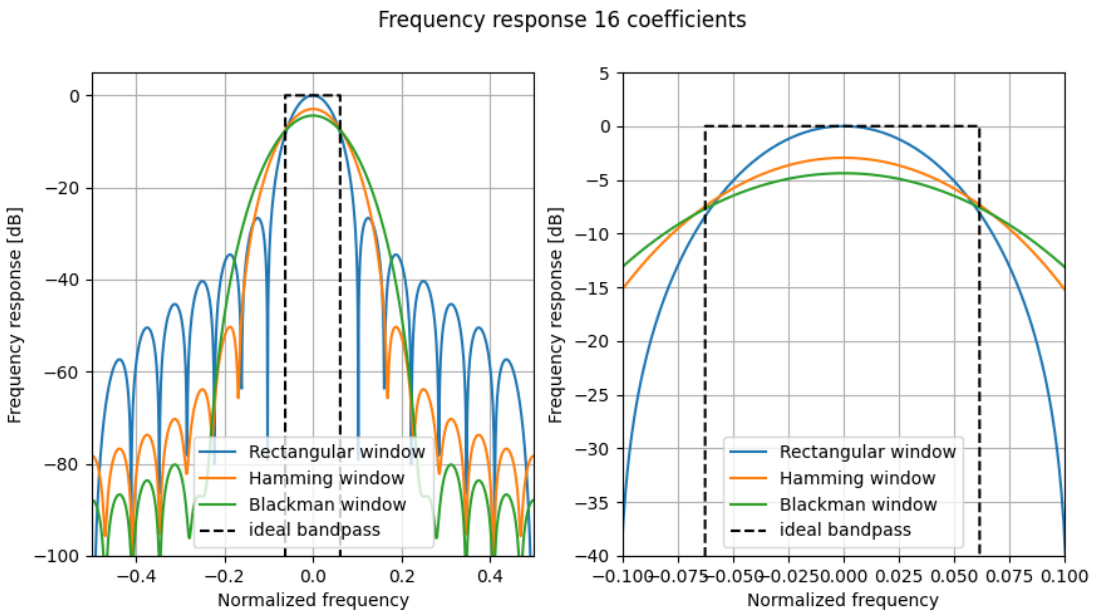
Spectrometer and bank of filters

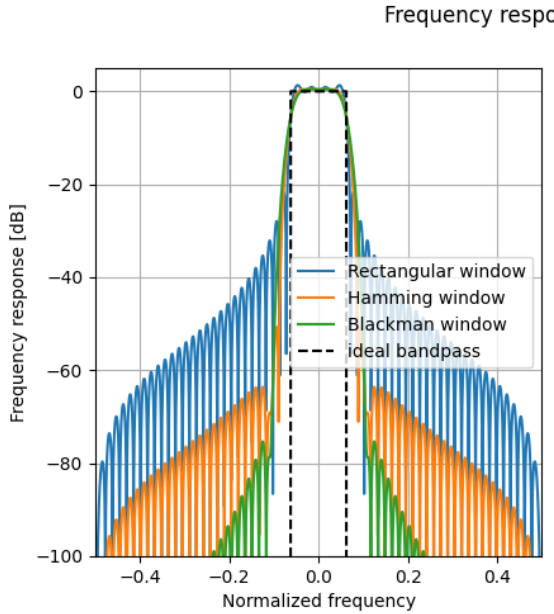
Model of a digital spectrometer

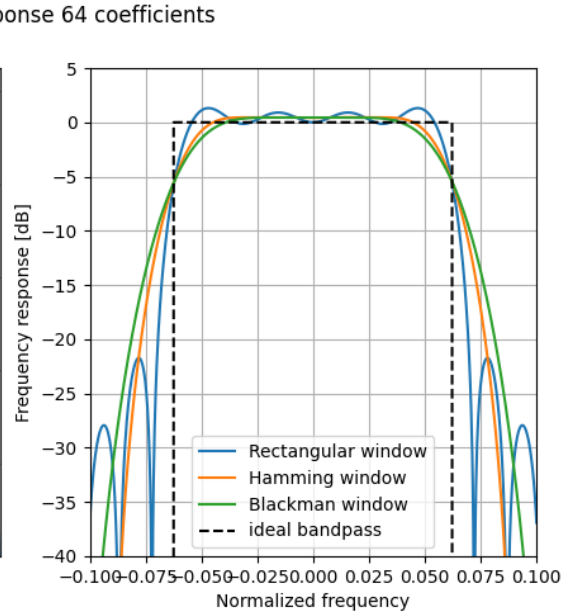


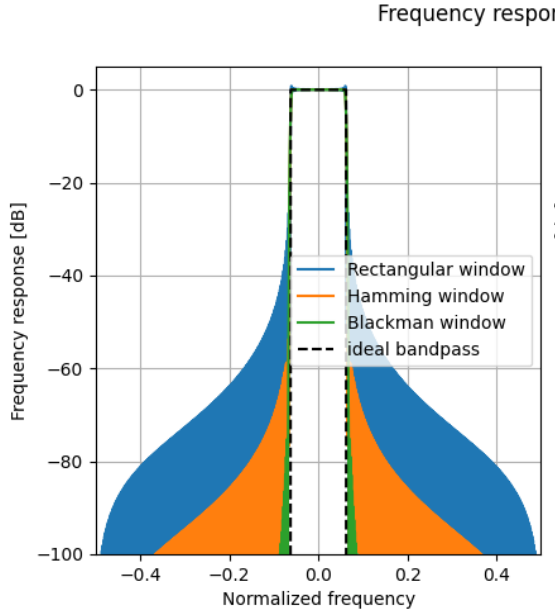
- z^i estimator of the mean of the power y^i over N samples $z^i[n] = \frac{1}{N}\sum_k \left| y^i[k] \right|^2$
- Goal: to have a definition of filter H^i with a good spectral resolution and a good variance of the power estimation while keeping a low computation complexity

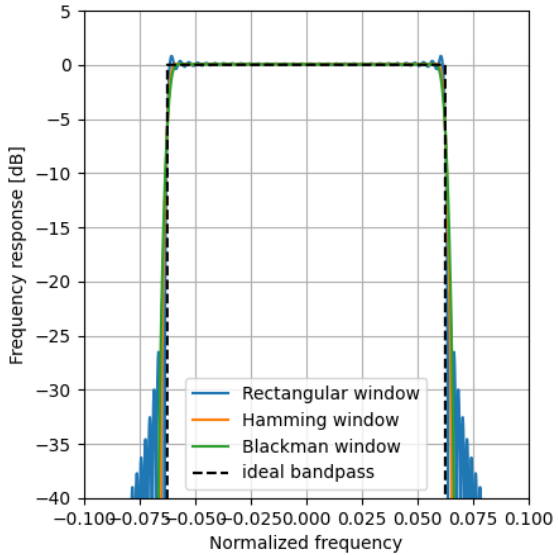
FIR filter response trade-off











Channel BW = Fs/16

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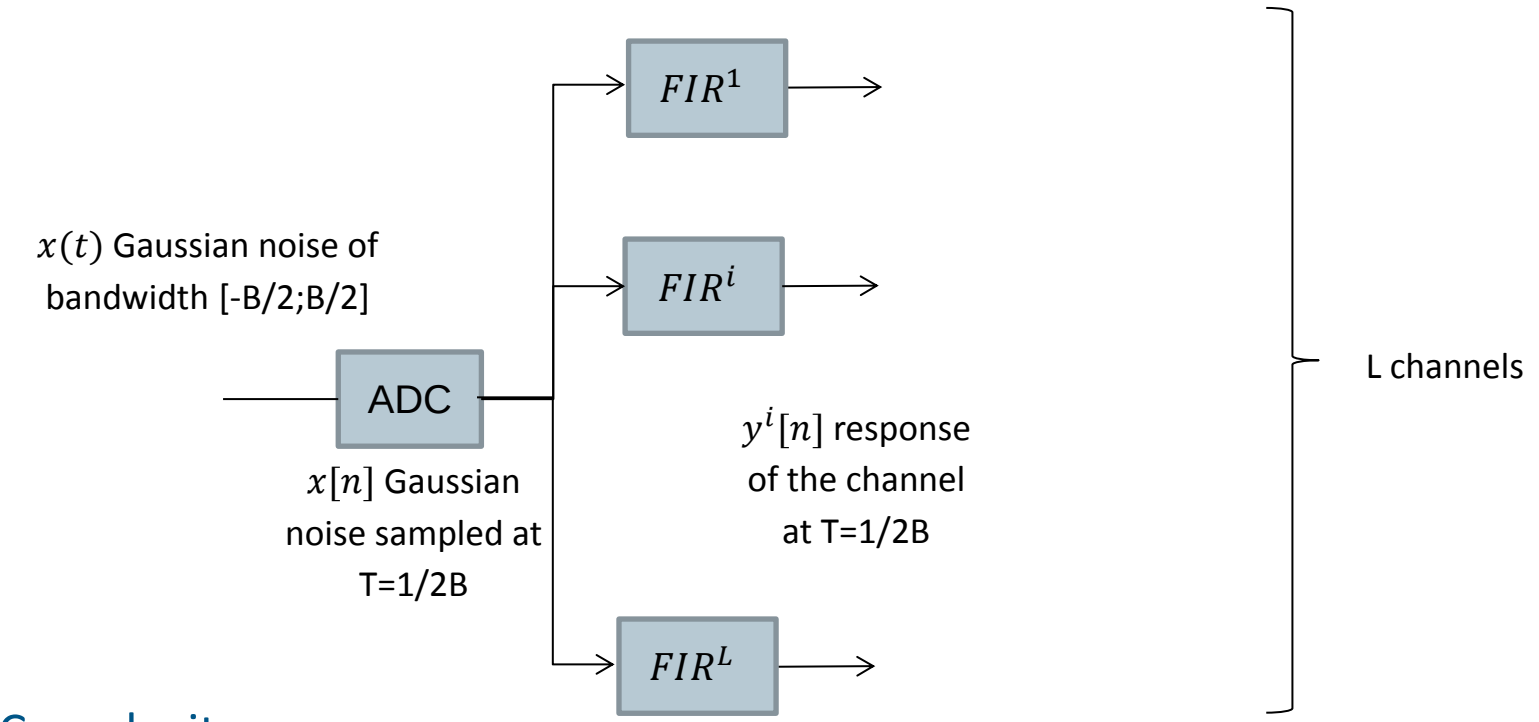
Filter architecture : Bank of FIR filters



- Computation Complexity
  - L filters
  - M coefficients per filter

    => L.M multiplications per input sample

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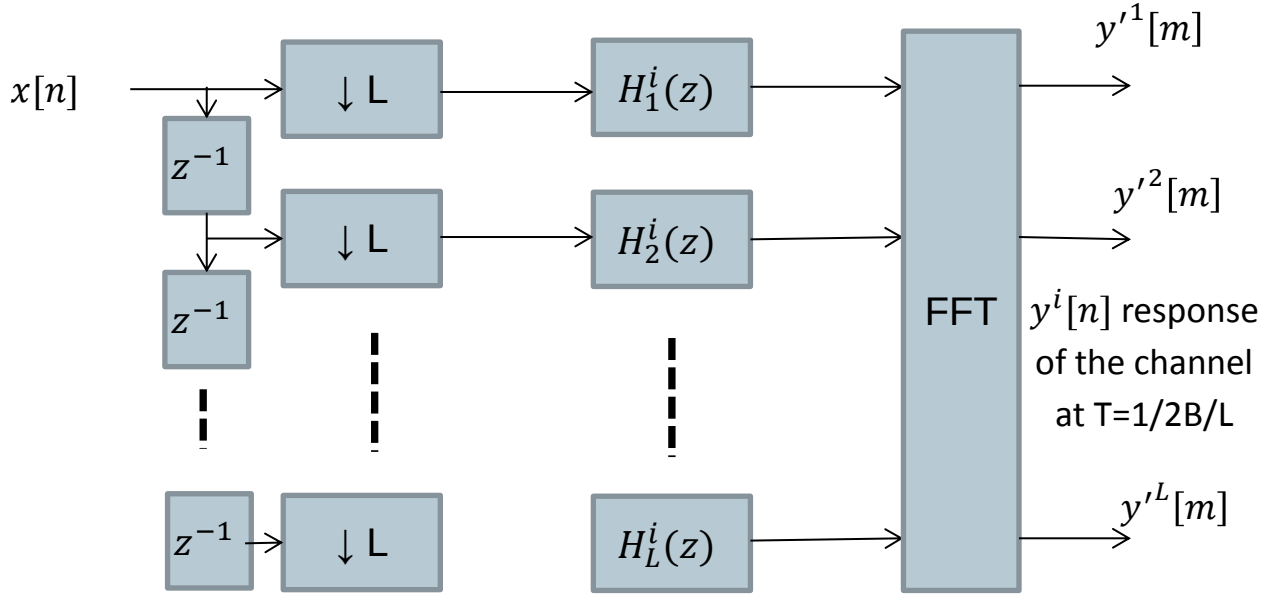
Filter architecture : Polyphase filterbank

- Uses FFT and polyphase filter architecture
  - Polyphase structure can be used to create a filter bank with low processing complexity
  - FFT is used to generate the L output channels in parallel



- Computation Complexity
  - M coefficient window
  - L prefilters with M/L coefficients, working at 1/L Fin
  - L point FFT, with L sample processed every L input samples

  $\frac{1}{L} * L * \frac{M}{L}$ multiplications per input sample for the prefilters

  $\frac{1}{L} .2L.log2(L)$ multiplications per input sample for the FFFT

  => $\frac{M}{L} + 2.log2(L)$ multiplications per input sample for the polyphase filterbank

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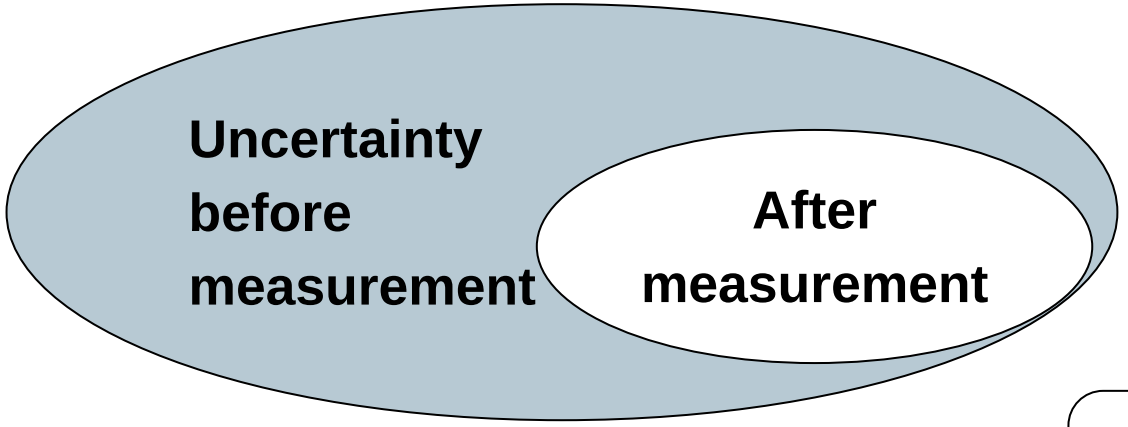
Filter architecture : High level analysis of computation complexity

	FIR filters in //	Polyphase filterbank	FFT
Number of Channels	L	L	L
Number of filter coefficients	M	M	0
Number of multiplications for L point inputs	LLM	M+2L.log2(L)	2L.log2(L)
Number of multiplications per input sample	LM	M/L+2.log2(L)	2.log2(L)
L=256, M=768	197k mult/sample	19 mult/sample	16 mult/sample

Number of channels and channel Bandwidth trade-off

Information content =

$$\log 2\left(\frac{area\ uncertainty\ before\ measurement}{area\ uncertainty\ aftermeasurement}\right)$$



	Bandwidth of a channel / sample rate (complex)					
Number of channels	0.1	0.5	1	1.5	2	4
8	2.14	2.44	**2.73**	2.63	2.42	1.76
16	2.26	2.74	**3.15**	2.80	2.54	1.84
32	2.22	2.88	**3.45**	2.98	2.69	1.93
64	2.09	2.90	**3.63**	3.15	2.86	2.05
128	1.99	2.91	**3.75**	3.28	2.99	2.14
256	1.99	2.93	**3.84**	3.36	3.07	2.19
512	2.05	2.92	**3.92**	3.41	3.11	2.22
1024	2.09	3.04	**3.98**	3.44	3.12	2.23

best when the channel bandwidth is equal to the channel spacing.

Limited gain over 256 channels

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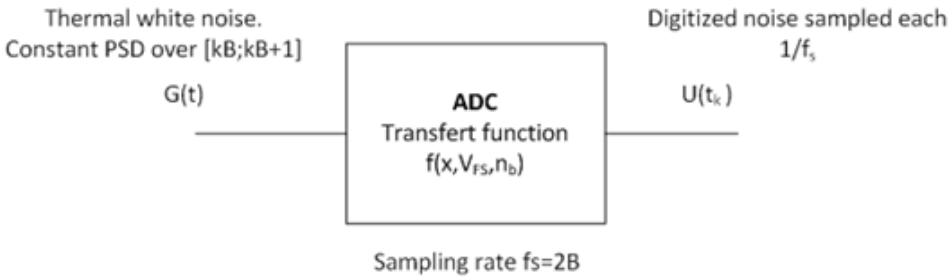
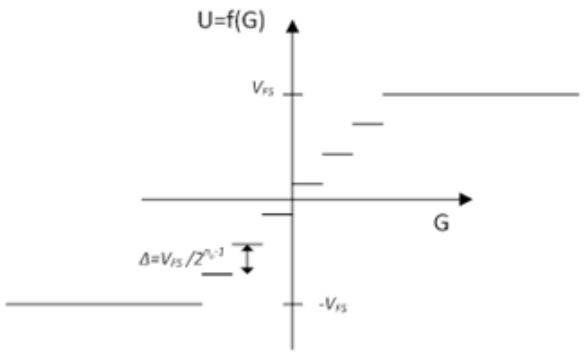
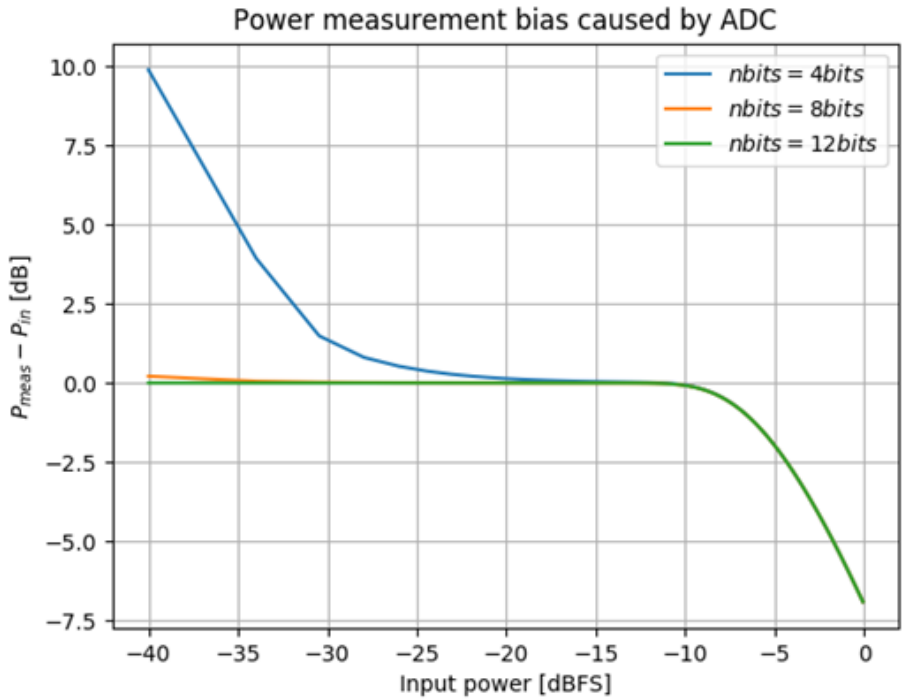
Impact of sampling quantization

- ADC quantization impact on measured power level depends on
  - Input signal back-off
  - ADC number of bits





f(x)=Δ ([x/Δ]+1/2)



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Breadboard Architecture

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Component selection for Breadboard

Parameters for the selection of FPGA and ADC

- Qualification to space environment of the component or an equivalent component
- Large ADC sampling rate (>6 Gsps, up to 20 Gsps)
- Power consumption per GHz
- Stable development tools and boards, usable immediately
- Export controls
- High RF bandwidth, to work in higher Nyquist bands

FPGAs candidates for Breadboard

		NG-ULTRA NX2H540TSC	ZYNQ Ultrascale+ RFSOC XQZU28DR	VERSAL AI CORE VC1902	RTG4 RT4G150	SPARTAN6 LX150	KINTEX XQRKU060
	Process	28nm FD SOI	16 nm FIN-FET	7nm FIN-FET	65nm Flash	45 nm	20 nm
	Radiation hardness	radhard	latchup sensitive	unknown	radhard	rad tolerant	rad tolerant
	Provider	NanoXplore	Xilinx	Xilinx	Microchip	Xilinx	Xilinx
	Type	SoC+FPGA	SoC+FPGA+RFADC	SOC+FPGA+NOC	FPGA only	FPGA only	FPGA only
SoC part (PS)							
	Architecture	ARMv8R	ARMv8A/V7R				
	Processing core(s)	4 x R52	4xA53 / 2xR5	2xA72 / 2xR5F			
FPGA part (PL)							
	FPGA technology	SRAM-based	SRAM-based	SRAM-based	Flash-based	SRAM-based	SRAM-based
	FPGA size - Total LUTs	537k LUTs	425k LUTs	900k LUTs	151k LUTs	147k LUTs	331k LUTs
	- Total LUTs (LUT4 equivalent)	537k LUTs	638k LUTs	1,350k LUT	151k LUTs	220k LUTs	497k LUTs
	Total DFFs	505k DFFs	851k DFFs	1,800k DFFs	151k DFFs	184k DFFs	663k DFFs
	DSP / Math blocks	1,344	4,272	1968	462	180	2,760
	RAM blocks (Mbit)	32 Mb	38 Mb	34 Mb	5.2 Mb	4.8 Mb	38 Mb
	HSSL SERDES (Gbps)	32@12.5Gbps	16@28Gbps	44@32.7Gbps	24@3Gbps	-	32@12.5Gbps
RFADC/DAC							
	RF ADC		8@4Gsps, 12bit				
	RF DAC		8@6.5Gsps, 14bit				
NOC / AI CORE							
	AI Cores			400@1,000 MHz			

Candidate with space grade equivalent

Other Candidate for ground breadboard

FPGA too small

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ADC candidates for breadboard

ADC RF	E2V EV12AQ600	TI ADC08DJ3200	TI ADC12DJ3200QML	TI ADC12DJ5200RF
Sampling Frequency	6.4 Gsps	6,4Gsps	6,4 Gsps	10,4 Gsps
Type	Interleaved SAR	Interleaved SAR	Interleaved SAR	Interleaved SAR
Quantization	12	8	12	12
Radiation hardness	Oui	Non	Oui	Non
Power consumption from datasheet	6.6 W	2,8 W	3 W	4 W
Interface Protocole #lanes@bitrate	ESIstream 8@12.8 Gbps	JESD204B 8@8 Gbps or 16@4 Gbps	JESD204B 8@12.8Gbps ou 16@6.4 Gbps	JESD204C 8@17.16Gbps ou 16@8.58 Gbps

Candidate with space equivalent part

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Preliminary analysis of power consumption and FPGA fill ratio (1/2)

Hypothesis

- 12.5 Gsample/s (~10 GHz Bandwidth)

- FFT256
- 12 bits in, 12 bin out, 64 samples per clock cycle.

- filterbank with 768 points window, 12 bits

- Power computation and accumulation,
  - 12 bits input
  - 36 bits output.

One instance at 195.3 MHz (Xilinx),

Two instances at 97.66 MHz (NG-Ultra).

	FFT256 64 sps/clk	Power + Accumulator	Polyphase Filter	others	HSSL Interface
CLB LUTs	32k	8k	16k	5k	14.8k
CLB Registers	34k	8k	16k	5k	13k
DSP	432	128	384	0	0
RAM18	128	128	0	0	0
serdes	0	0	0	0	2*8@12.5 Gbps

Required ressources in Xilinx KU060 for the preliminary analysis

Preliminary analysis of power consumption and FPGA fill ratio (2/2)

Remarks :

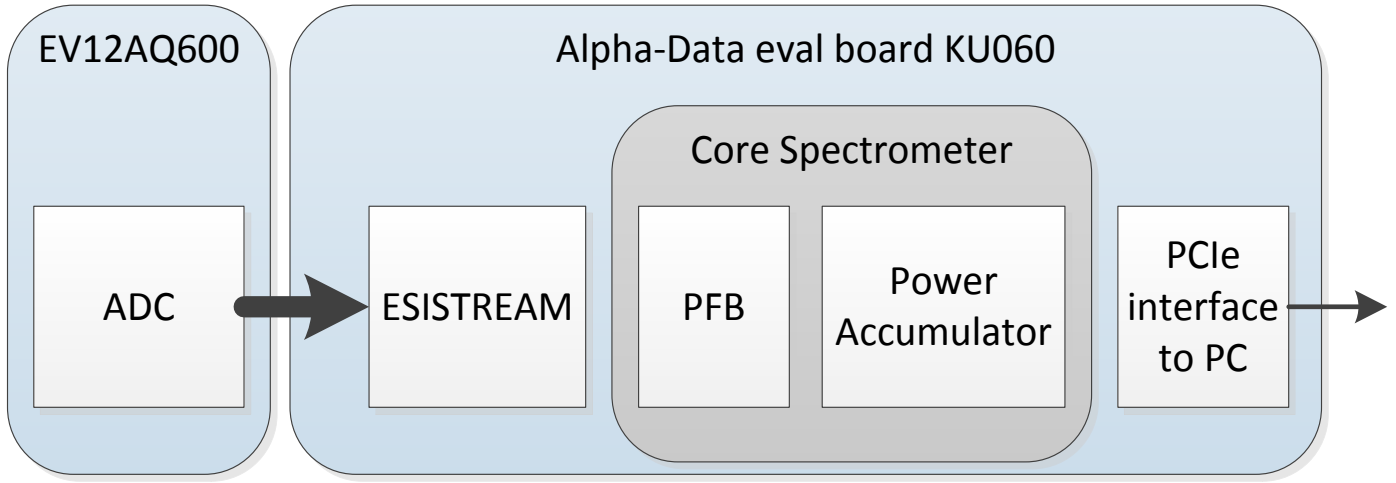
- *NG-Ultra is too small for 2 instances*
- *Zynq Ultrascale plus RFSOC power consumption includes integrated ADC. Very efficient system level consumption.*
- *VERSAL AI Core power consumption is based on preliminary power estimator.*
- *VC1902 has a number of LUT and DFF much larger than needed, leading to large power consumption for this use case.*

	XQ Zynq UltraScale+ RFSoC	Space-grade Kintex UltraScale	VERSAL AI CORE	NG-Ultra
	XQ ZU28DR	XQR KU060	VC1902	NX2H540T SC
FPGA freq. used	195.3 MHz	195.3 MHz	195.3 MHz	97.65 MHz
Power estimate	10.1 W	10.4 W	18.4W with AI Cores 17.5W only FPGA	12.1 W
RF ADC included	Yes	No	No	No
DSP use	22%	34%	48%	140%
LUT use	14%	23%	7%	42%
DFF use	7%	11%	3%	30%
BRAM use	12%	12%	13%	76%

Breadboard architecture

Breadboarding goals

- Representative power measurement on hardware
- Develop and debug digital signal processing code
- Precise evaluation of processing resources
- Develop and validate on a representative device the calibration and measurement strategy



Hardware Architecture:

- KU060 evaluation board
- EV12AQ600 FMC evaluation board

- Maximum bandwidth: 3.2 GHz of RF bandwidth (x2 if 2 ADC are used)

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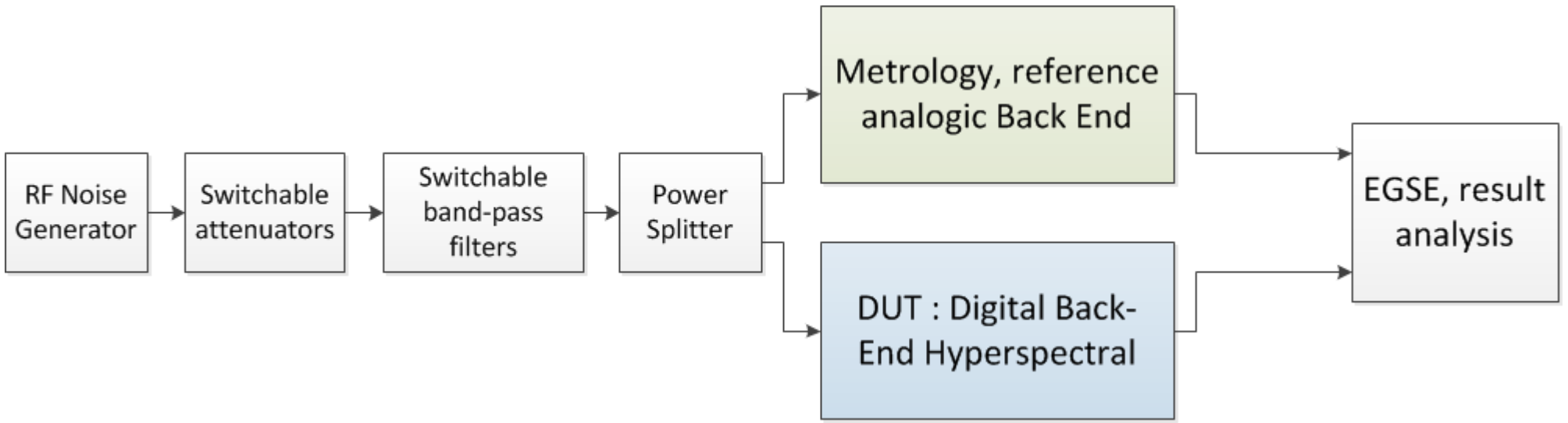
Test setup

- No RF generator can meet the required radiometric bias(0.1K)

⇒ Back-end hyperspectral is measured against a reference Analogic Back-end

- Switchable attenuators and band-pass filters are used to simulate the input signal



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Test measurements

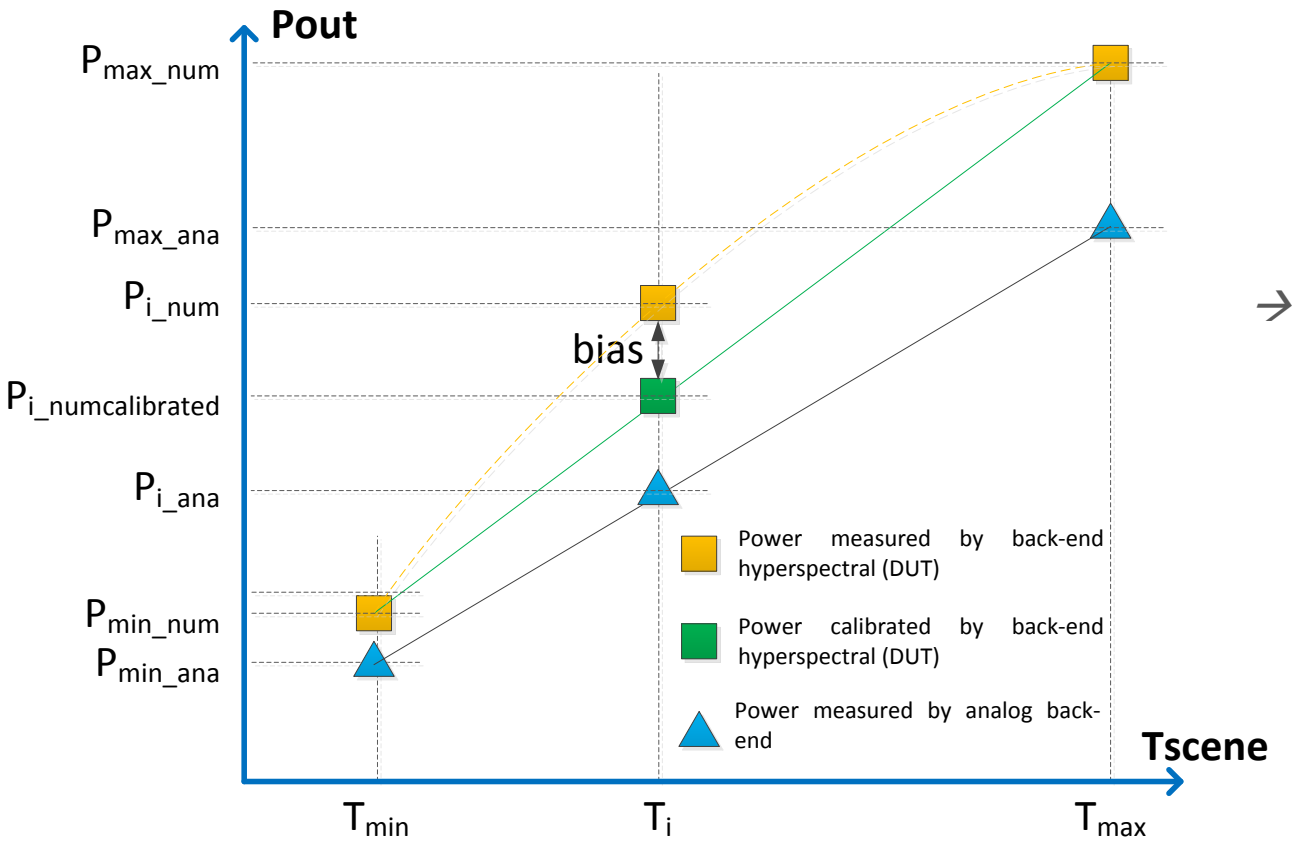
- Radiometric Bias
  - It is the error between the measured power and the calibrated power.

$$P_{i\_numcalibrated} = P_{i\_ana} \times \frac{P_{min\_num}}{P_{min\_ana}}$$

$$Relative\ Error_{\%} = \frac{Bias}{\Delta P}$$

$$Bias = P_{i\_num} - P_{i\_numcalibrated}$$

$$\Delta P = P_{max\_num} - P_{min\_num}$$



→ *Measure to perform with optimum integration time*

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Conclusions