GOMX-5 APPS - THE ADVANCED PAYLOAD PROCESSORS FOR THE GOMX-5 IOD MISSION

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1 ABSTRACT

The Advanced Payload Processors (APPs) was developed targeting in-orbit demonstration (IOD) in the GOMX-5 mission. GOMX-5 is a flight demonstration for next generation cubesat missions, which will demand advanced attitude control, large processing capabilities, and high throughput data exchange between space and ground segments. APPs was jointly conceived by Gaisler in Sweden, GMV and CBK in Poland, and UFSC in Brazil, in order to demonstrate multiple processing technologies developed within ESA activities. APPs is a 1U size payload with five stacked boards supported by a mechanical structure and interconnecting interfaces, eventually to be integrated as one of the payload modules in the 12U GOMX-5 satellite developed by Gomspace, Denmark. The APPs payload consists of one GNSS RF front-end and a DPU from GMV/CBK, one BRAVE board from UFSC based on NanoXplore's NG-Large FPGA, one multi-processor GR716 board from Gaisler, supervised by the fault-tolerant GR716 microcontroller, and one GR740 board, based on the fault-tolerant GR740 processor, acting as a controller and main S/C interface for the entire APPs cube. The boards will be used for various experiments related to features such as GNSSW receiver, radiation detection, higher-performance processing and FPGA reconfiguration.

2 INTRODUCTION

This paper describes the "GOMX-5 Advanced Payload Processors Development" (GOMX-5 APPs) activity and the current status of the development. The activity was started in November 2020 and is part of the "GOMX-5 IOD CubeSat Mission Implementation – Phase C/D" mission, with the aims to validate technologies and capabilities enabling deployment and operations of commercial nanosatellite constellations. Specifically, the mission objective is to:

- Flight-demonstrate on one 12U nanosatellite platform the next generation of nanosatellite constellation-related technologies including:
    - Compact RF transceivers
    - Compact optical instruments for Earth observation (EO)
    - On-board propulsion providing high total delta-v
    - GNSS precise position pointing
    - Combination of hardware and software solutions to increase in-orbit reliability and availability for the system

This space segment (part of the mission architecture) is composed by a single spacecraft based on the GomSpace's 12U platform. The spacecraft will carry different payloads based on the selection carried out by ESA and GomSpace. The GOMX-5 platform shall be capable of accommodating secondary technology demonstrator payloads identified, traded-off and selected in conjunction between ESA and GomSpace. The APPs team has been selected by ESA and GomSpace to provide the APPs Payload module.

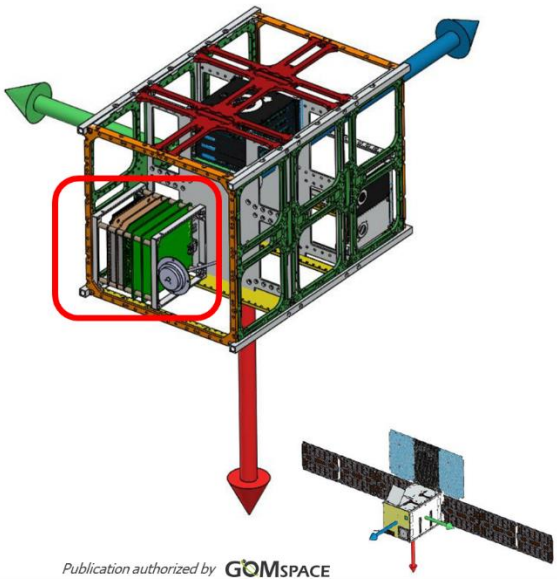


Figure 1 GOMX-5 platform with APPs

The main objective for the APPs activity is to demonstrate multiple processing technologies developed within ESA activities and acquire flight heritage from related components by means of

- Combination of processors and reconfigurable logic in APPs allowing for multiple IOD experiments.
- Realization in the Advanced Payload Processors (APPs) 1U size payload module

The activity is operated under an informal consortium consisting of the organizations, together with support from the Microelectronics section at ESA:

- Cobham Gaisler AB, Göteborg, Sweden

- CBK / PAN, Warsaw, Poland
- GMV Innovating Solutions, Warsaw, Poland
- Space Technology Research Laboratory, UFSC, Florianópolis, Brazil.

The organization structure and responsibilities for the main parts of the APPs module is illustrated in Figure 2 below.

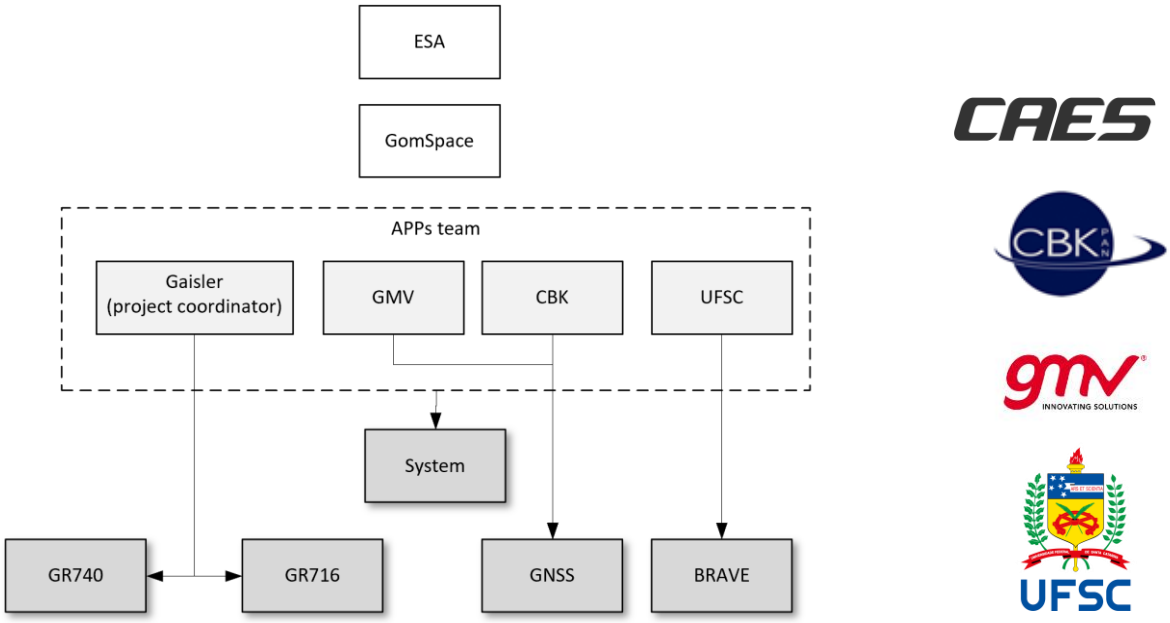


Figure 2 Organzation and main responsibilities

The activity has previously been presented in June 2021 [1] and November 2021 [2].

3 APPS DESIGN

The APPs cube is illustrated in Figure 3 below.

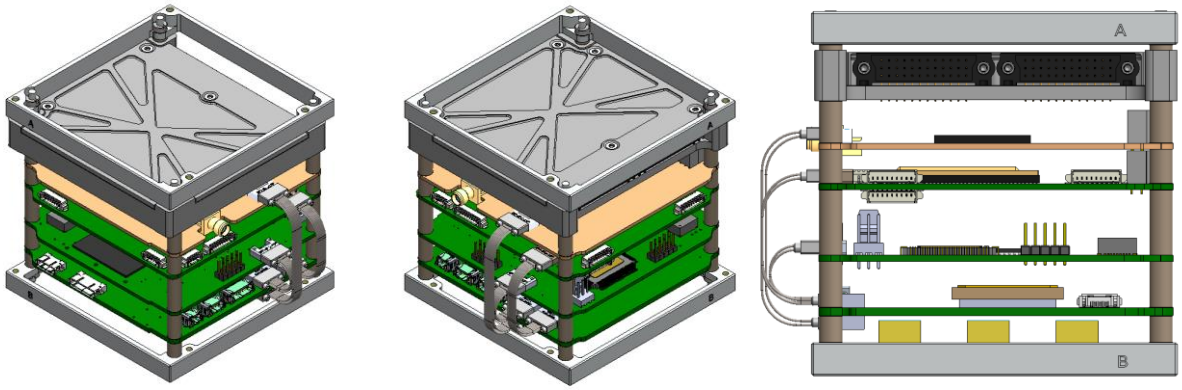


Figure 3 APPs design

Apart from the mechanics and interconnecting cables, it consists of the following five boards, from top, with abbreviated board names and brief explanation of features:

- GNSS Digital - Processor part of GNSS Software Defined Receiver
- GNSS RF Frontend - RF frontend part of GNSS Software Defined Receiver
- BRAVE - Reconfigurable NG-Large FPGA supported by microcontroller

- GR716 - Microcontroller accompanied by co-processor (LEON5/NOEL-V demonstrator) and radiation sensor
- GR740 - High performance processor, APPs cube controller, power and communication router

The system architecture is illustrated in Figure 4 below.

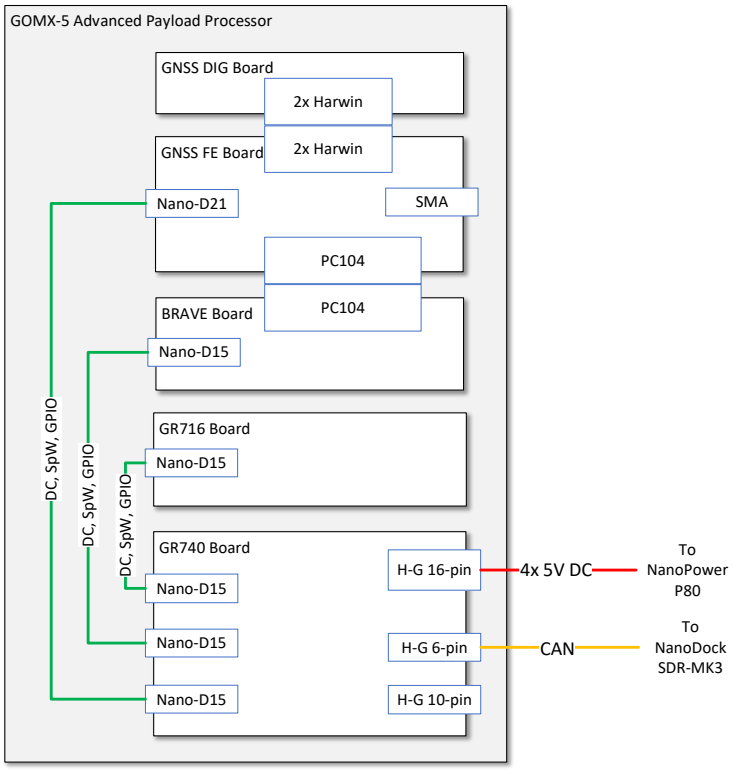


Figure 4 APPs system architecture

All communication with the spacecraft is handled through the GR740 board using a CAN bus interface. The same applies for the physical connection of the four supply lines, routed directly through the GR740 board.

The components or design solutions being subject to the main objective of acquiring flight heritage are following, distributed over the five boards:

- GR740 LEON4-Quad-Core Processor
- GR716 LEON3 Microcontroller
- NOEL-V / LEON5 Test Chip
- NanoXplore (BRAVE) NG-Large FPGA
- GNSS Front-End
- GNSS Software Receivers on GR740 and Zynq 7030

The board design, components and related experiments are described further below.

4 APPS GR740 BOARD

The architecture and implementation are illustrated in Figure 5 below.

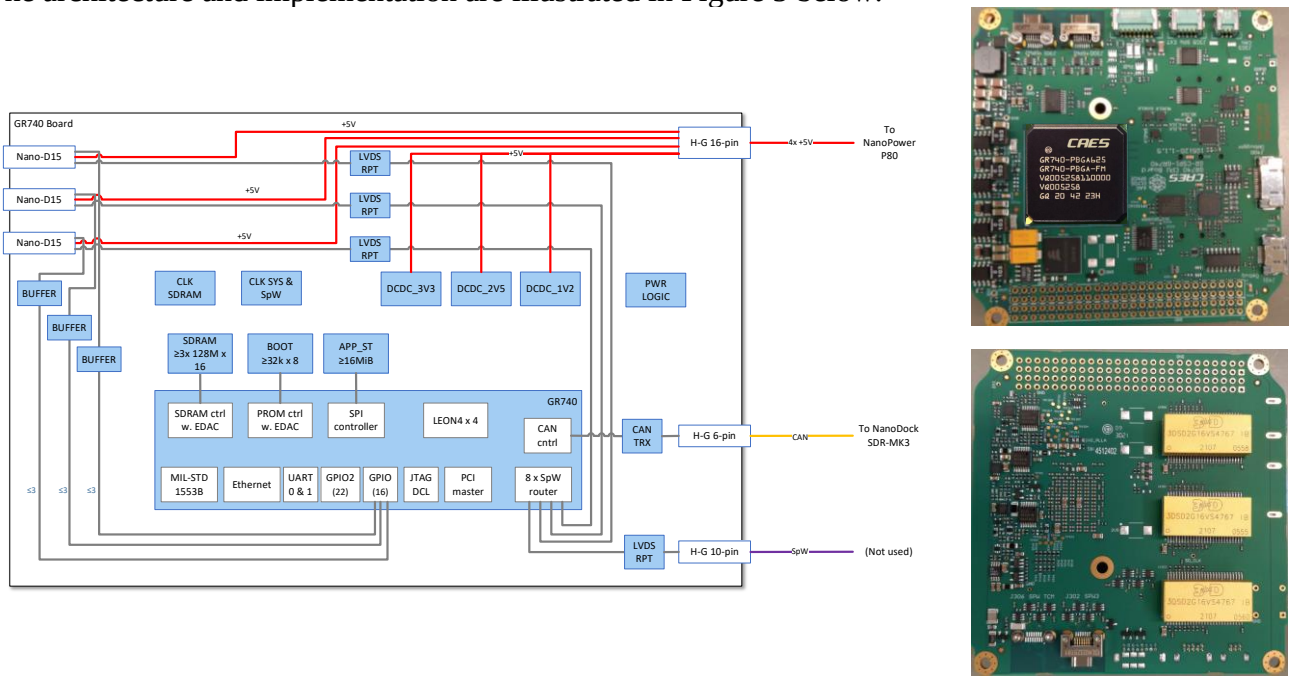


Figure 5 GR740 board

The GR740 processor [3] is the main part of the GR740 board. It interfaces to the spacecraft via a CAN interface, and via the internal SpaceWire router it connects to the other boards. There are also GPIO signals which the GR740 can use to control basic features of the other boards, such as controlling hardware resets. One of the 4 channels of the DC input supply is used on the GR740, but the three others are routed though the board, without any control by the GR740.

The component subject to acquiring flight heritage is the plastic variant of the radiation-hard quad-core fault-tolerant LEON4 SPARC V8 processor targeting space constellations. It has the same functionality, fault-tolerance and radiation-hardness as the GR740 system-on-chip device in ceramic package. It is available as a Plastic Ball Grid Array (PBGA) with 625 balls. Footprint is compatible the GR740 Ceramic Column Grid Array (CCGA).

Figure 6 GR740-PBGA625

5 APPS GR716 BOARD

The architecture and implementation are illustrated in Figure 7 below.

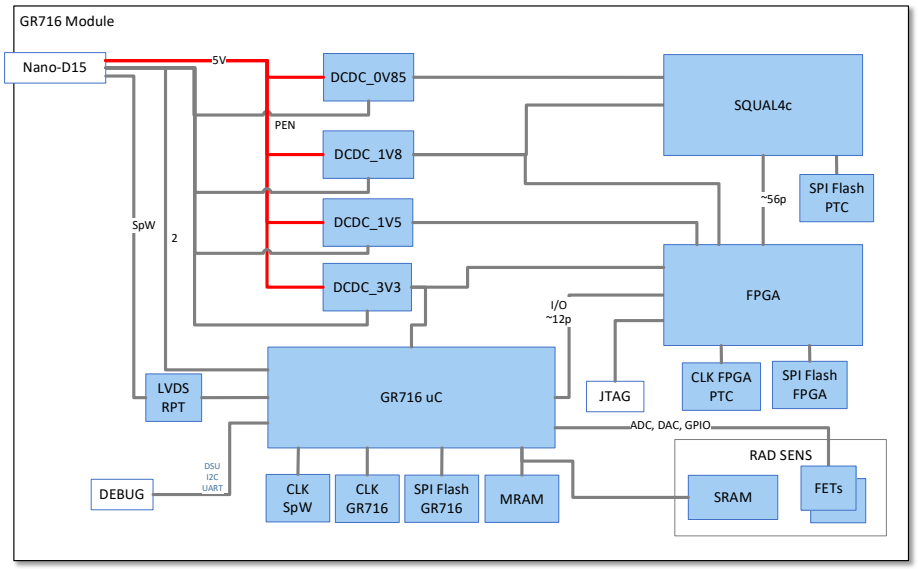
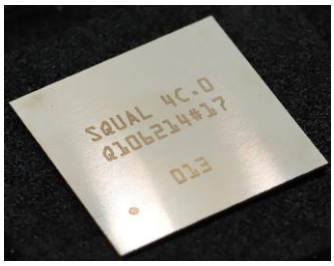


Figure 7 GR716 board

The GR716 microcontroller [4] is the main controller of the GR716 board and communicates with the GR740 board. There are also two other main blocks used for different experiments, one being a high-performance LEON5/NOEL-V demonstrator chip (SQUAL4c) and one block containing parts used as radiation sensors.

The components specifically being subject to acquiring flight heritage are the GR716 microcontroller and the LEON5/NOEL-V demonstrator chip. The latter includes rad-hard demonstrators implemented as a LEON5FT SPARC V8 32-bit processor and a NOEL-V RISC-V on silicon proven on STM 28nm GEO P2. In addition, a third component, the GR54LVDS054PZ Quad LVDS Buffer/Repeater is included in the board. It has a dedicated design for SpaceWire interfacing, packaged in a 25-pad ceramic land grid array package, and radiation hard >300 krad (Si), SEL and SEE immune.



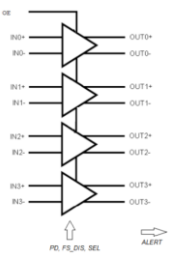


Figure 8 Components on GR716 board

6 APPS BRAVE BOARD

The architecture and implementation are illustrated in Figure 9 below.

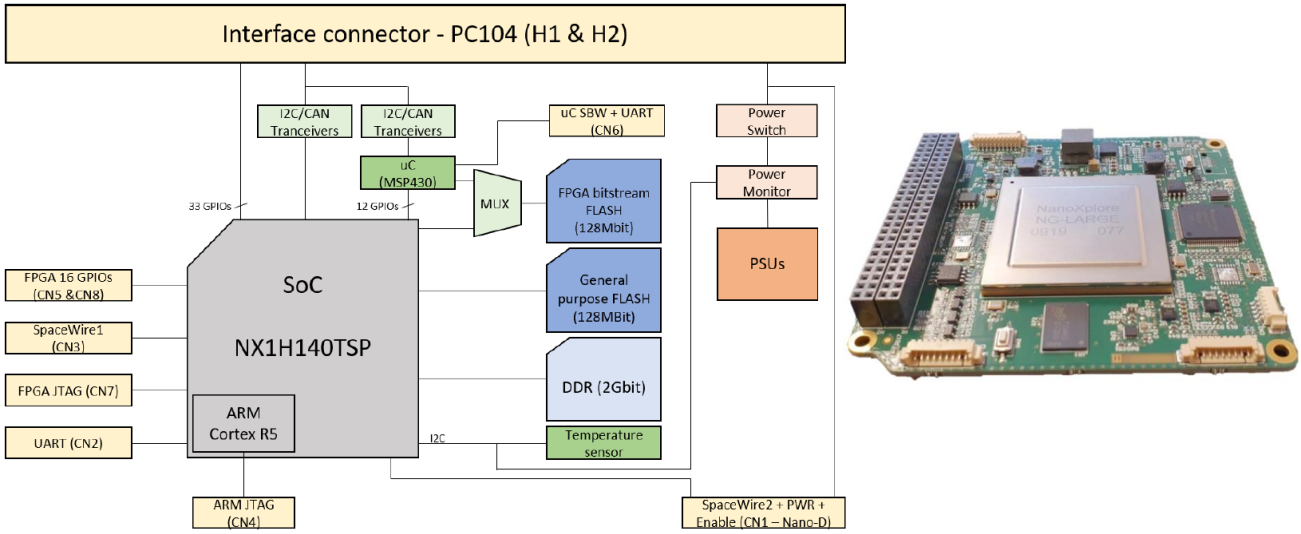


Figure 9 BRAVE board

The NG-LARGE NX1H140TSP FPGA (BRAVE FPGA) from NanoXplore [5] is the main component of the BRAVE board. It is a mid-end RHBD SRAM-based FPGA manufactured on 65 nm STM C65-SPACE process technology developed to be used in harsh environments applications.

The major idea behind the BRAVE board development is providing a platform capable of integrating in the same board the processing units responsible to perform several outer space experiments. Complementary, the system can perform successive reconfigurations of the FPGA during its operation, just receiving new bit-streams via up-link communication. Due to its capability and flexibility, such platform can be used as the core for a wide range of applications and missions. A minimal telemetry package is always provided since the main goal is to validate the operation and resilience of the BRAVE FPGA device.

Moreover, an auxiliary processor, the microcontroller MSP430-FR6989, is assembled with the BRAVE board, in order to provide the in-orbit reconfiguration feature. This feature is not required for the BRAVE board operation, but increases the system's overall reliability, as it can operate in case of a critical failure (as a fallback recovery).

7 APPS GNSS BOARDS

The architecture and implementation are illustrated in Figure 10 below.

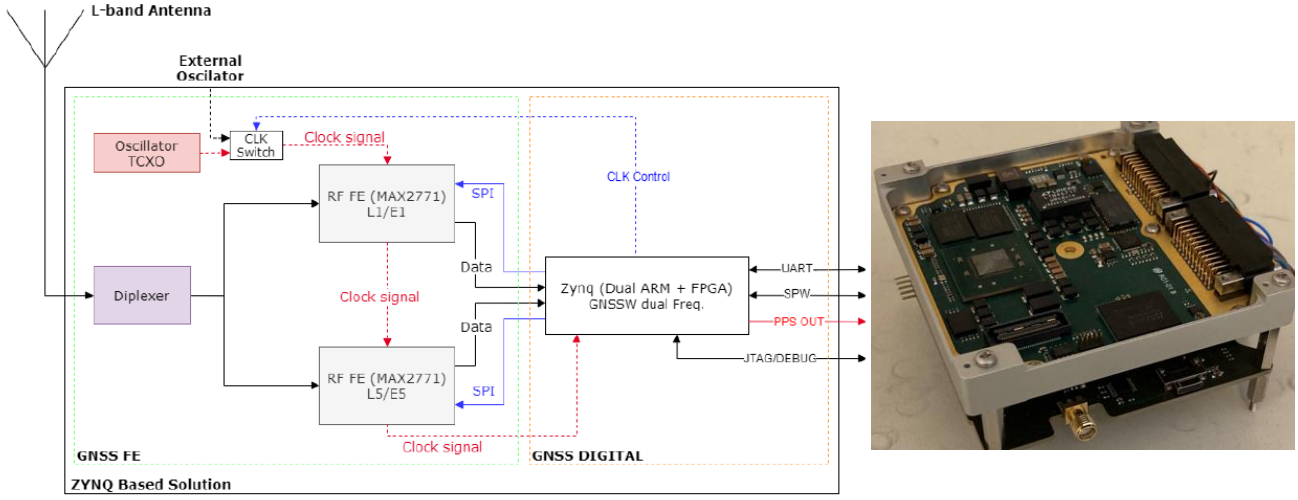


Figure 10 GNSS boards

The GNSSW Receiver consists of two main blocks interconnected via Harwin connectors:

- The GNSS Digital Board, consisting of Dual ARM® Cortex-A9 MPU [6] with built-in FPGA (optional used for eventual HW accelerations for GNSS digital signal processing) used as control and Digital Processing Unit (DPU) in the GNSS SW payload. The GNSS Digital Board will be equipped with:
  - hardware interfaces to connect with GNSS FE board (Harwin connectors)
  - drivers/receivers for SpW (Harwin connectors)
  - serial link for realization of communication with external systems (PC104 like) – in case of APPs it will be used to connect with the Brave Board.
  - For executing GNSS receiver with utilization of GR740 module, TM/TC link and fast data transfer link will be implemented via SpW.
- The GNSS FE Board. The RF signal will be provided to this module by one SMA connector from one dual frequency GNSS antenna. Through diplexer the FE module will accommodate two separate signal sampling chains to be ready for HW redundancy or dual frequency sampling. The main role of FE module is receiving and conditioning of GNSS signal, as also down converting L1 and/or L5 band to baseband and realization of sampling process.

In addition to local GNSS operation, the GNSS boards are also connected to:

- The BRAVE board via a PC104-alike connector, and
- The GR740 board via a 21 pin Nano-d connector.

This design provides high performance and flexibility with respect to utilization of microprocessor and FPGA resources. It provides possibilities to perform GNSS experiments using the GNSS boards alone, or in combination with one or both of the BRAVE and GR740 boards (where dedicated cores will in that case be used for the GNSS experiments).

For the GNSSW Receiver, acquirement of flight heritage is focusing on the entire concept, rather than specific components.

8 OBJECTIVES AND EXPERIMENTS

The experiments will be conducted by payload consortium and GomSpace (as operator) with the support of ESA. The consortium is responsible for the experiment configurations and for analysis of the received data and experiments results. GomSpace as an operator is responsible for maintaining the communication with the satellite and its defined orientation during the experiments. See illustration below.

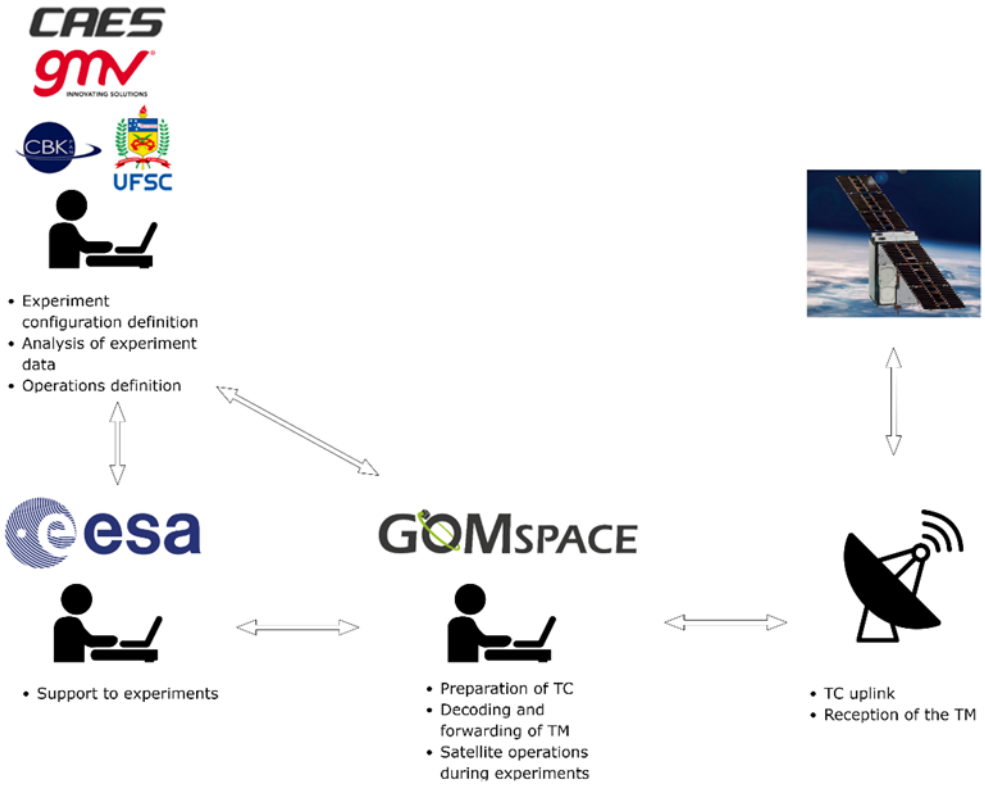


Figure 11 Experiments operational flow

The table below summarizes the experiments of the APPs module. It is divided into three parts, separated by the individually numbered ID's, for three submodules each:

- GNSSW – for GNSS Receiver related experiments
- CG – for Gaisler experiments
- US – for UFSC experiments

Table 1 Summary of the APPs experiments

#	ID	Experiment	Scope	Prel. duration
1	GNSSW-01	GNSSW mono frequency receiver on GR740	The experiment focuses on testing the mono frequency (E1/L1) receiver running on LEON4 processor with different SW configurations.	A few days
2	GNSSW-02	GNSSW dual frequency receiver on ZYNQ	The experiment focuses on testing the dual frequency (E1/L1+E5/L5) receiver running on LEON4 processor with different SW configurations.	A few days
3	GNSSW-03	GNSSW single frequency receiver on ZYNQ	The experiment focuses on testing the single frequency (E1/L1) receiver running on Zynq processor with different SW configurations.	A few days

#	ID	Experiment	Scope	Prel. duration
4	GNSSW-04	GNSSW mono frequency receiver on GR740 with Brave as samples distributor	The experiment focuses on testing the single frequency (E1/L1) receiver running on GR740 processor with Brave board as samples distributor. BRAVE will also host a hardware FFT-based GNSS fast acquisition unit.	A few days
5	APP-01	Gaisler multi-experiment	Perform all sub-experiments/applications on the GR740 and GR716 boards. Includes TMC, housekeeping, memory scrubbing, FPGA demonstration and SEU detection on multiple chips.	Sequences spread out over mission
6	APP-01LD	Gaisler - long duration	Long duration radiation experiments. SEU on CERN SRAM and TID measured. (The devices must be biased all the time when subject to radiation, for correct data).	Full mission duration
7	UF-01	FPGA Reconfiguration	The experiment focuses on testing the reception of a new file from the ground station.	A few days (week) spread out
8	UF-02	New FPGA bitstream upload	The experiment focuses on reconfiguring the BRAVE FPGA with a new file received from a ground station (UF-01).	A few days (week) spread out
9	UF-03	FPGA Algorithm	This experiment focuses on checking the memories health.	A few days (weeks) spread out
10	UF-04	FPGA Algorithm	The experiment focuses on testing the encryption and decryption of the data sent to and received from the GR740.	A few days (weeks) spread out

The detailed planning of durations and slots is currently on-going, coordinated by GomSpace, based on the power consumption and available power during different modes and for all the payloads in the satellite. The total duration for the part of the mission being subject to most of the experiments above, as well as for the other payloads, is six months long.

9 TEST CAMPAIGN

The APPs has been subject to an extensive test campaign. Apart from local board and software tests performed by each partner, there have been integration tests performed on the complete or parts of the stack, focusing on the communication and interaction between the boards. Some of these have been performed at ESTEC, and some on any of the partner's sites, often in combination with remote control and supervision by the other parts. These integration tests are as by April 2022 still on-going but completed to an extent allowing for an EM (Evaluation Model) delivery of the APPs stack to GomSpace for further spacecraft integration and testing.

In addition, an EQM (Evaluation Qualification Model) of the APPs stack has been subject to environmental testing on qualification levels. The environmental tests have consisted of vibration tests, thermal vacuum tests and EMC tests, with a first phase completed at the ESTEC facilities, see photos below.

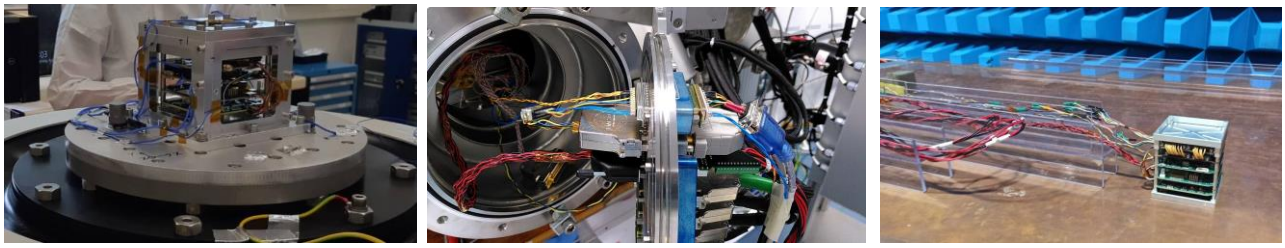


Figure 12 Environmental test setup (mechanical, thermal-vacumm), EMC

The EQM setup illustrated to the left in Figure 12 includes the surrounding test fixture. The mechanical tests target the “GEVS profile” as defined in [7]. A first test campaign has been performed. Refinement of the mechanical support structure is on-going, and a follow-up test campaign is planned.

Thermal vacuum tests have also been performed on the EQM on qualification levels with a test profile specified as in the figure below. There have been no concerns observed related to these tests and no additional tests are foreseen needed on qualification levels.

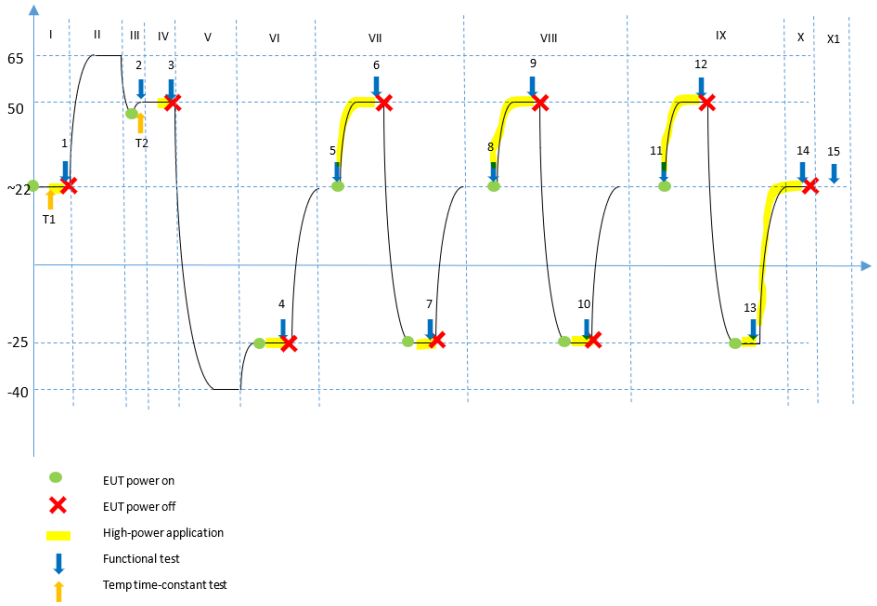


Figure 13 Thermal vacum test profile

EMC tests have also been performed at ESTEC in all four areas of radiated and conducted emission and susceptibility tests. Some minor anomalies have been observed, found to be related to a non-representative power supply input lead setup. No re-design or repeated tests on qualification levels are foreseen due to this.

10 CONCLUSION

As per April 2022, the GOMX-5 APPs module has been developed and tested using EM and EQM boards. A delivery of a partially completed EM stack to GomSpace is planned during April, for tests as part of a flat-sat configuration. Further parallel iterations of the APPs functionality and software should be considered as a consequence of flat-sat integration testing. Continued work is on-going in parallel to adjust the mechanics, including a follow-up test campaign. Preparation of Flight Model (FM) variants of the boards is also on-going with various progress. Some of the APPs FM boards exists, but some have not yet been assembled.

11 REFERENCES

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