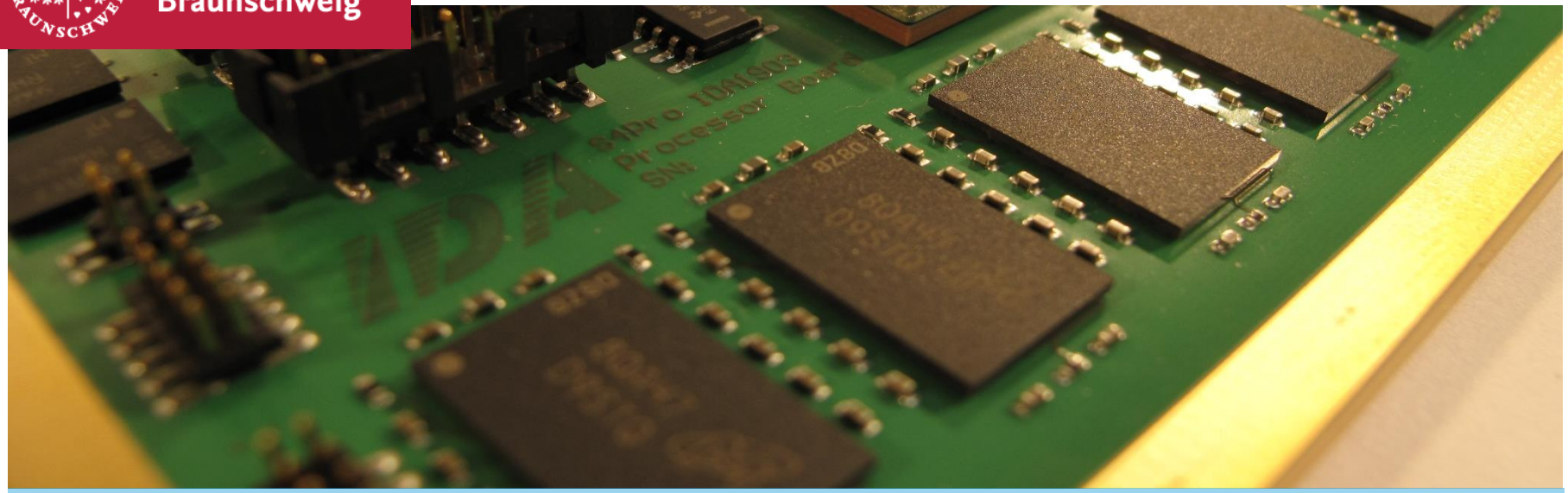
Technische Universität Braunschweig

INSTITUTE OF COMPUTER AND NETWORK ENGINEERING



Performant and Flexible On-Board Processing Modules Using Reconfigurable FPGAs

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Introduction and Motivation

- Ever increasing data amount needs to be transferred and processed
- Downlink telemetry rate of space-crafts is still very limited

➡ High demands for on-board processing power, while low resources consumption remains a constraint.

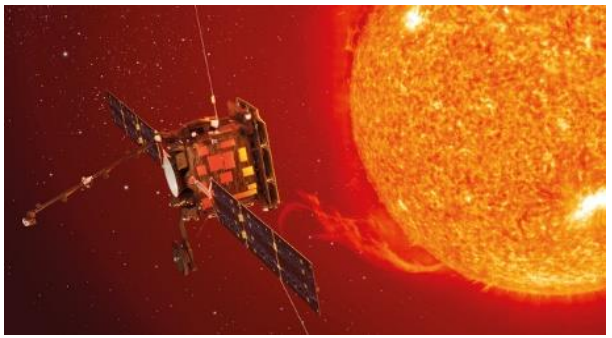
Solution:

➢ In-flight dynamically reconfigurable SRAM-based FPGAs

- Enhancement of on-board processing with unprecedented levels of operational flexibility
- **Adaptation** of the system regarding functional and fault-tolerance requirements, improving both, performance and maintenance.
- FPGAs combines the performance of a hardware implementation with the flexibility of software realization

Example:

Solar Orbiter Mission

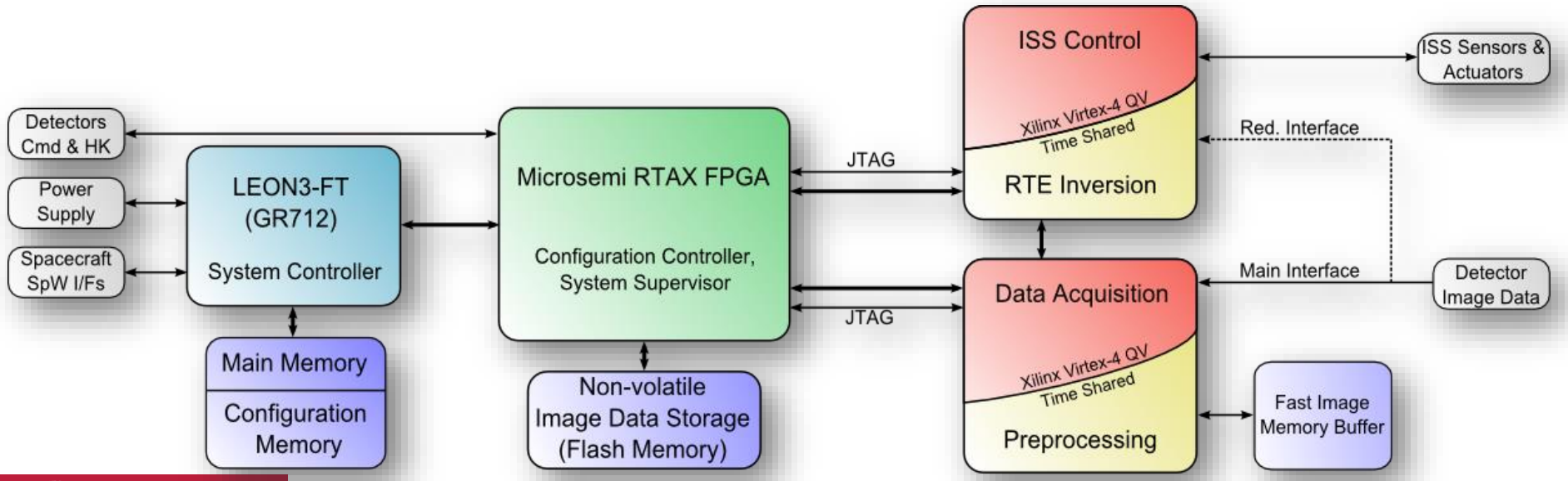


Source: ESA mission website
http://sci.esa.int/solar-orbiter/55750-artists-impression-of-solar-orbiter/

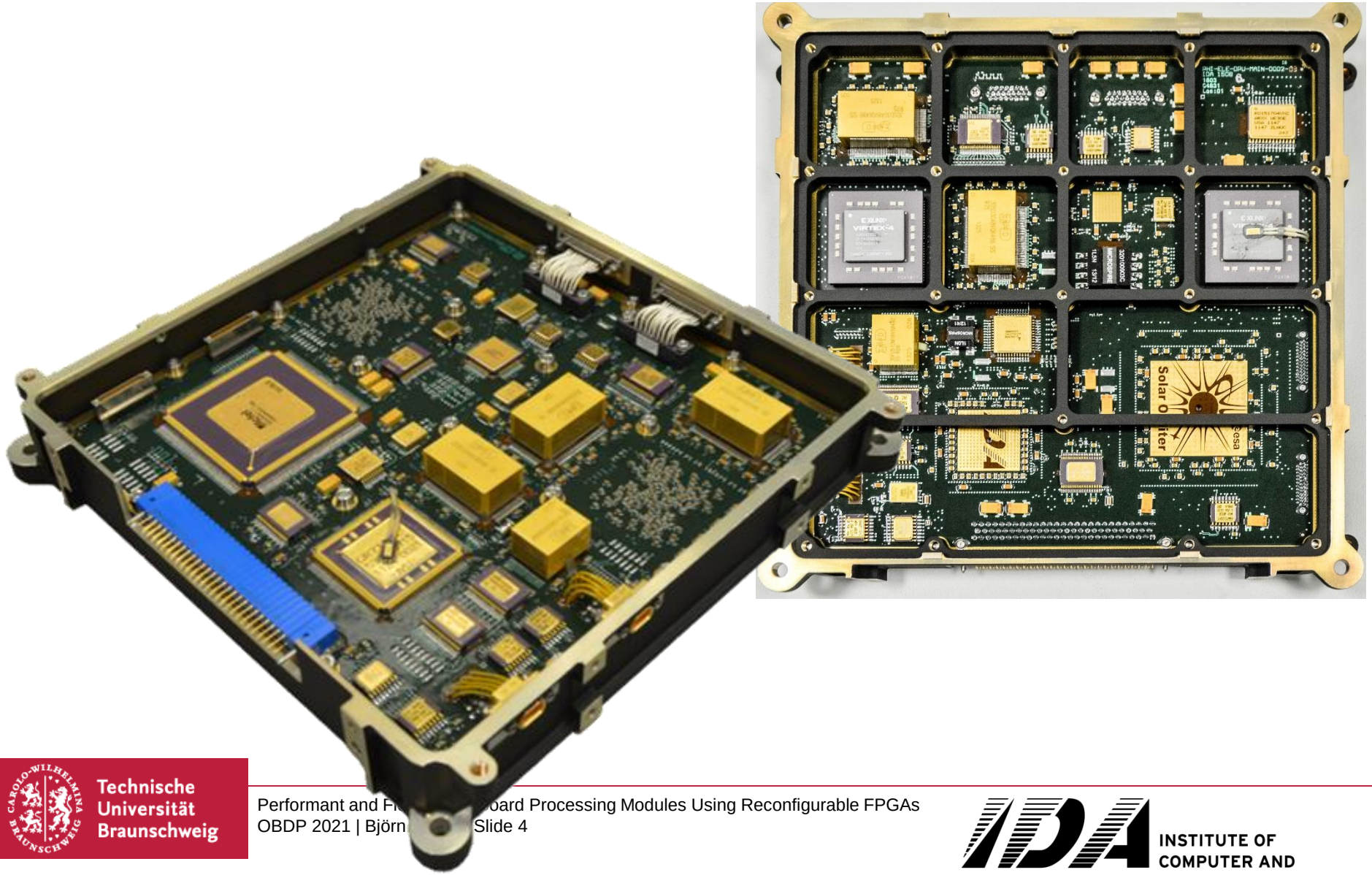
Solar Orbiter PHI Data Processing Module

In-flight SW and HW adaptation:

- Maximize use of resource limited HW platforms
- Based on space-qualified Xilinx Virtex-4 SX55 FPGAs
- Flexible, in-flight reconfigurable, radiation-tolerant
- But only fixed, ground verified configurations

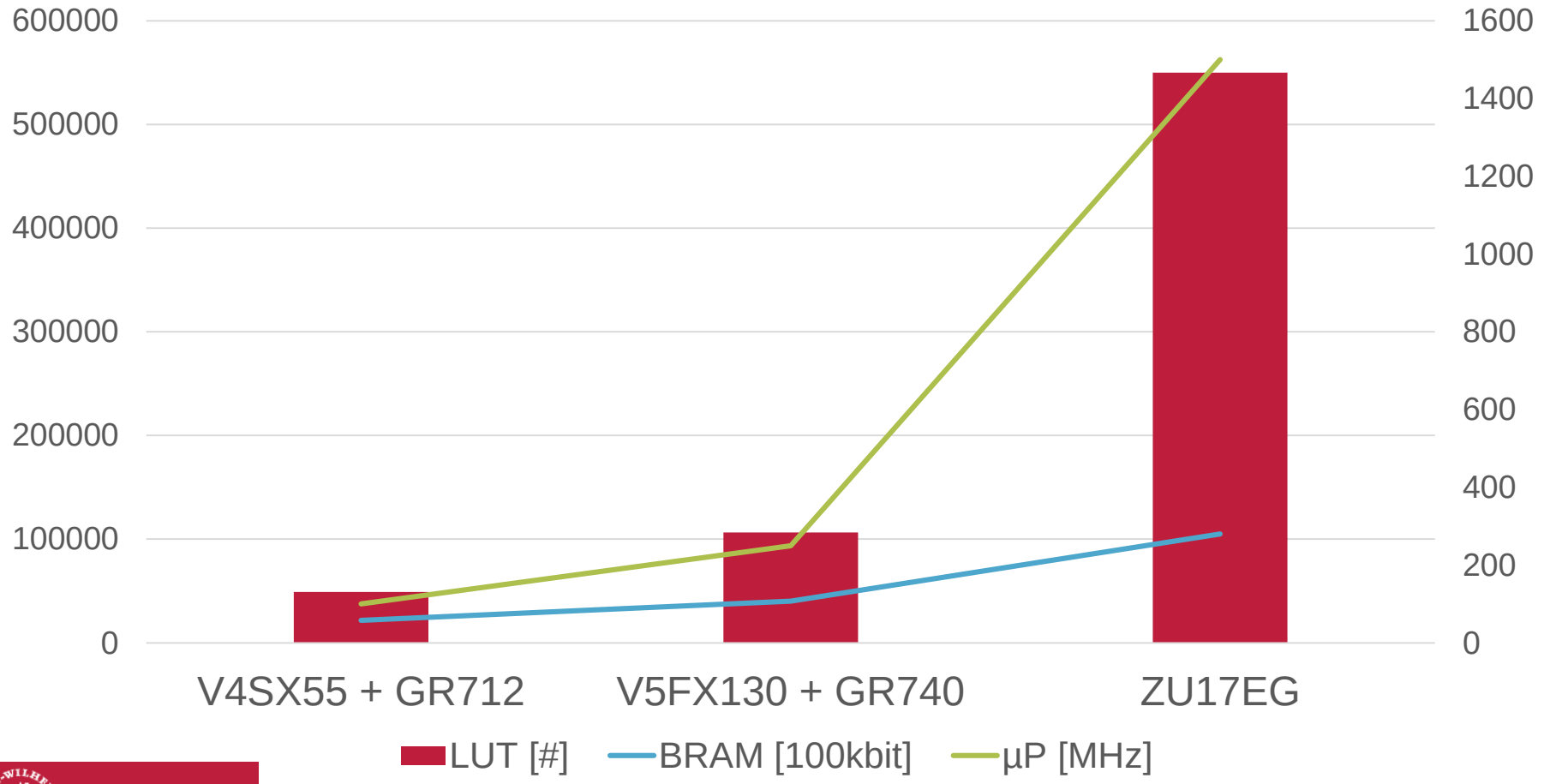


Solar Orbiter PHI Data Processing Module



Resources and Speed

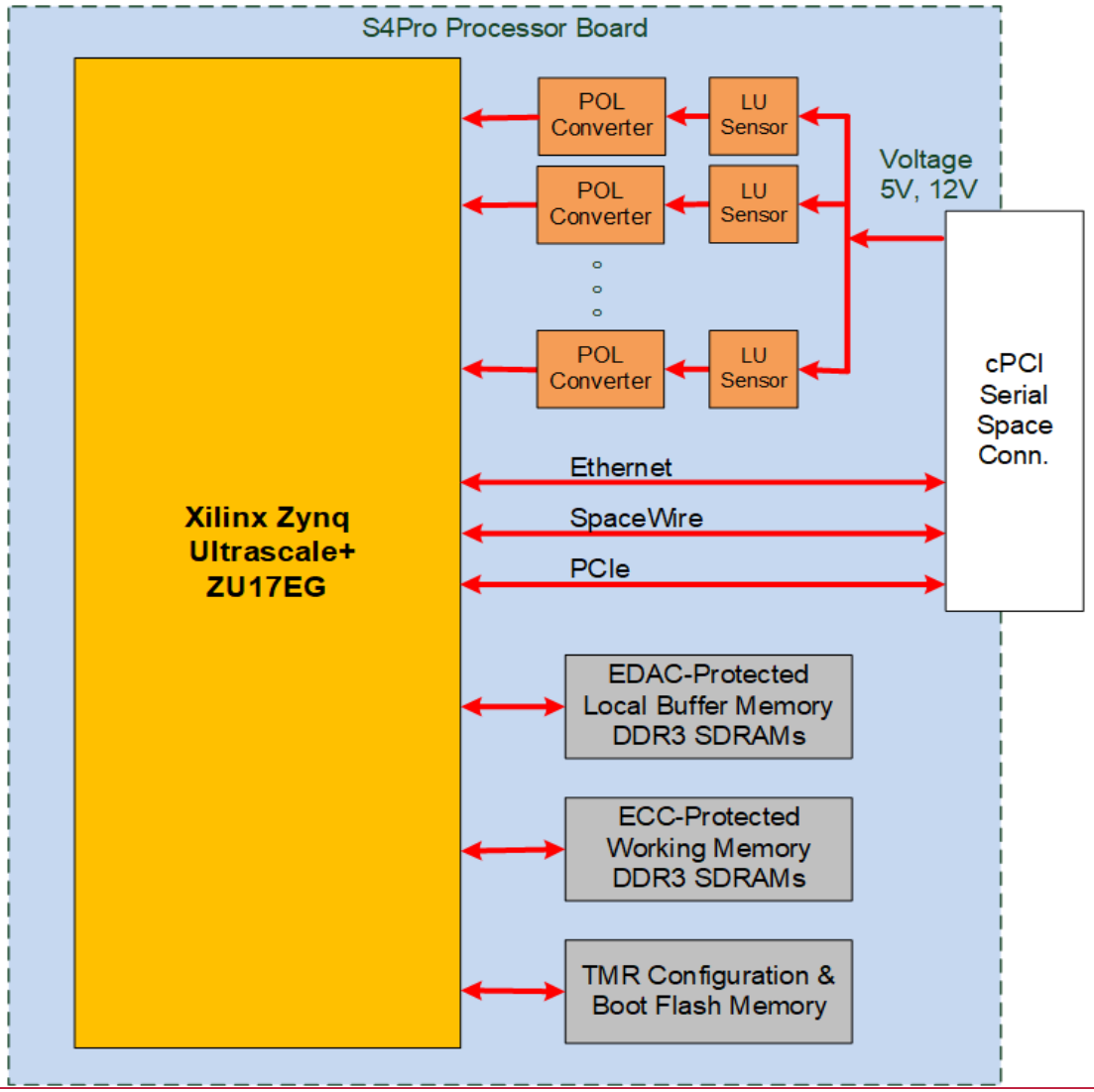
Comparison: Xilinx Virtex-4/5 systems with state-of-the-art Zynq Ultrascale+



Universal Processing Module

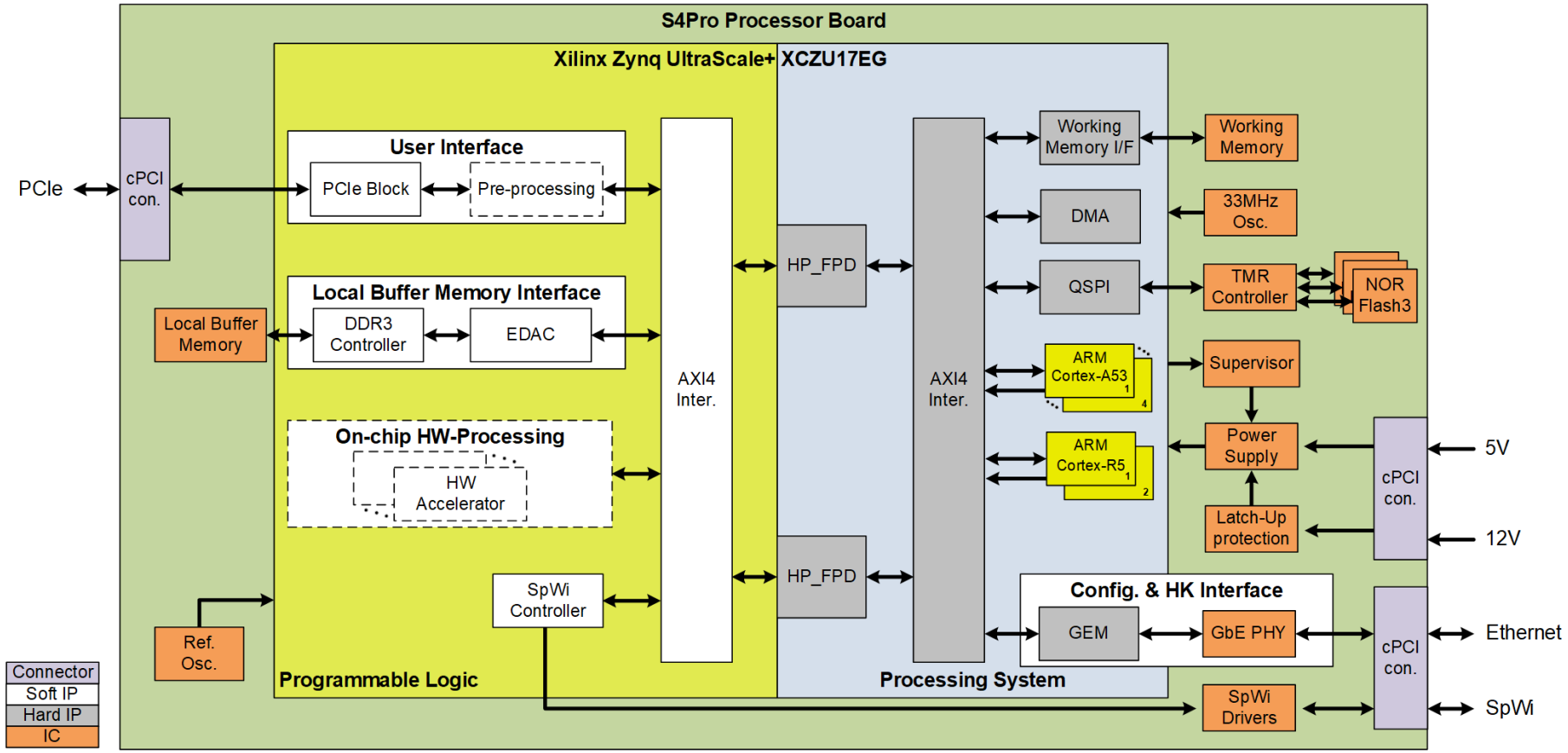
Xilinx Zynq Ultrascale+ MPSoC device:

- state-of-the-art
- cPCI Serial Space standard
- used in **S4Pro** for high performance payload processing
- throughput of tens of Gbit/s
- tightly coupled (multi)-processor-FPGA SoC
- sequential execution of processing pipelines by concurrent change using dynamic partial reconfiguration



Controlling Concurrent Change

Processing Module Architecture



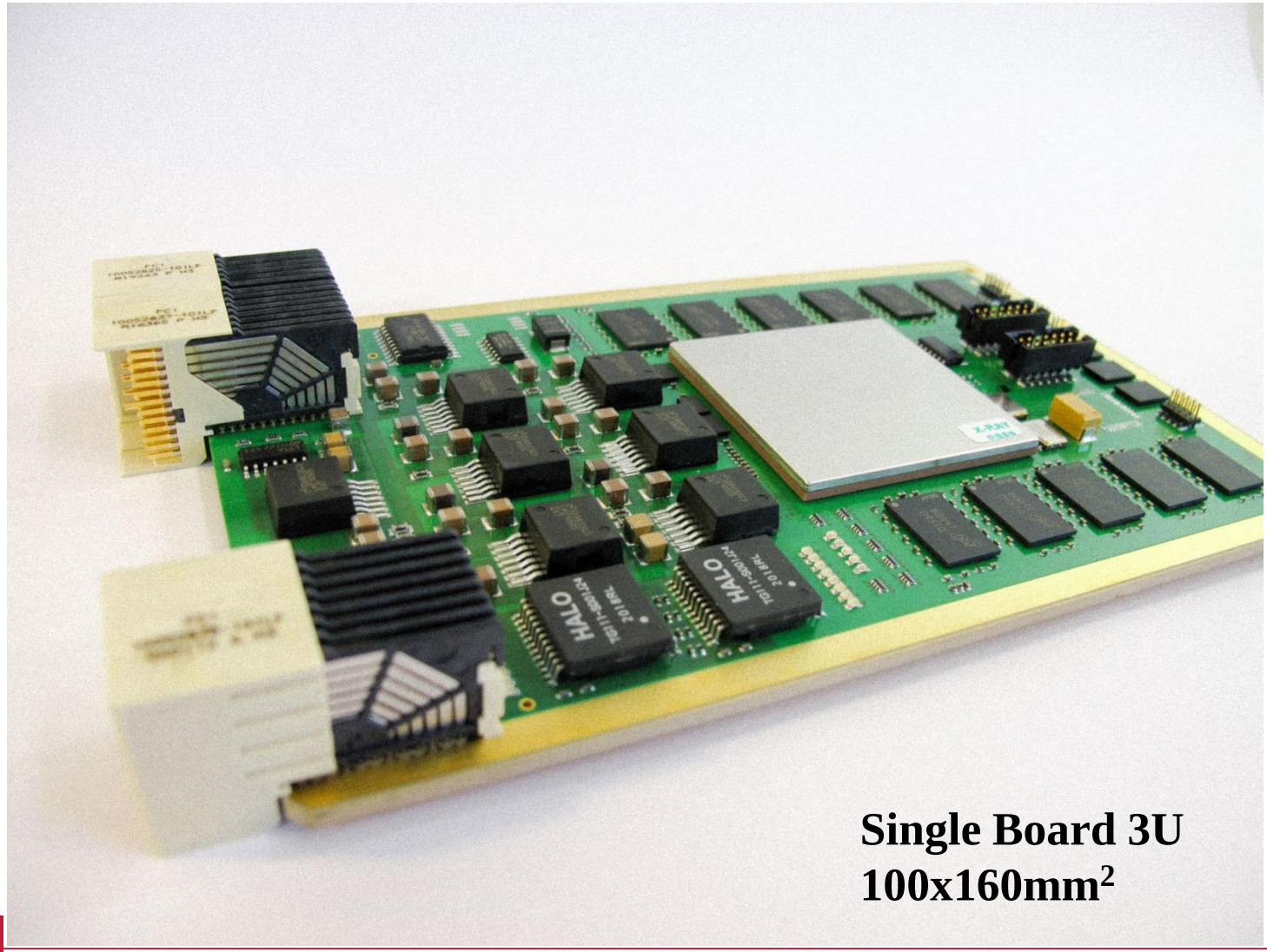
Processing Module Details

- Buffer (PL) and working (PS) memory:
  2x ECC-protected 64 Gibit DDR3-SDRAM (user capacity)
- FPGA configuration and user software: 2 Gibit NOR flash memory with TMR
- High-speed IF: 8-lane PCIe 2.0 with optional pre-processing block
- General-purpose IF: Dual SpaceWire
- Configuration & HK IF: Dual Gigabit Ethernet controller (GEM) and PHY (10/100/1000 Mbit/s)
- Debug: JTAG & UART

Data Rates:

- PCIe 2.0 block data throughput up to 32 Gbit/s per direction
- Buffer memory, 64-bit net data bus, 400 MHz, burst data rate up to 51.2 Gbit/s
- Working memory, 64-bit data width, 600 MHz, burst data rate up to 76.8 Gbit/s
- AXI interconnects, 150 MHz, burst data rate up to 76.8 Gbit/s

Processing Board



Improved Reliability against SEEs

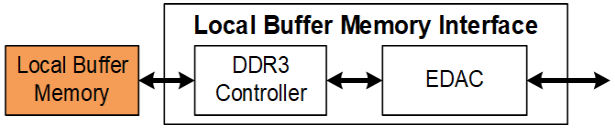
- Board based on industrial COTS parts
- DDR3 Memory error correction
- Boot process is crucial: TMR NOR flash memory and dedicated controller
- Power supply: High-accuracy POL power modules, measurement & control logic to detect SEL overcurrent
- Rad-hard supervisor: Monitor by watchdog, power cycle

- FPGA configuration scrubbing essential, but does not prevent SEUs:
  - TMR mitigation for critical datapath and control modules needed
  - But mitigation may not be needed for data processing:
    - ✓ Regular test with test vectors, correct FPGA configuration, re-process again

DDR3 Memory Error Correction

PL buffer memory:

- DDR3 SDRAM EDAC is based on NGMMA
- Reed-Solomon RS (12, 8) scheme, correction of two symbol (8 bit/symbol) errors
- 12 DDR3 SDRAM devices (512M16) needed for 64+32 Gibit



PS working memory:

- Hard-wired Hamming code based EDAC block
- Double-bit error detection, single-bit error corr.
- 10 DDR3 SDRAM devices (512M16) needed for 64+8 Gibit

➢ Periodical memory scrubbing to mitigate SEUs

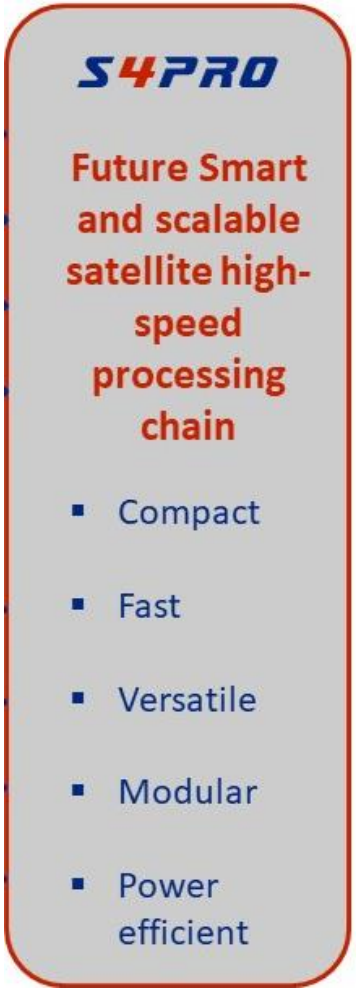
➢ Software conditioning to handle device SEFIs without data loss

S4Pro Overview

H2020 project S4Pro
(Smart and Scalable Satellite High-Speed Processing chain)

- Combine state-of-the-art industrial computing technologies (Xilinx Zynq UltraScale+) and space qualified embedded computing platforms (Gaisler GR740)
- Optimize data processing chain, e.g. for SAR and multispectral imaging applications
- On-board high performance payload processing and storage for institutional missions
- Technology transfer to nano- and small satellites

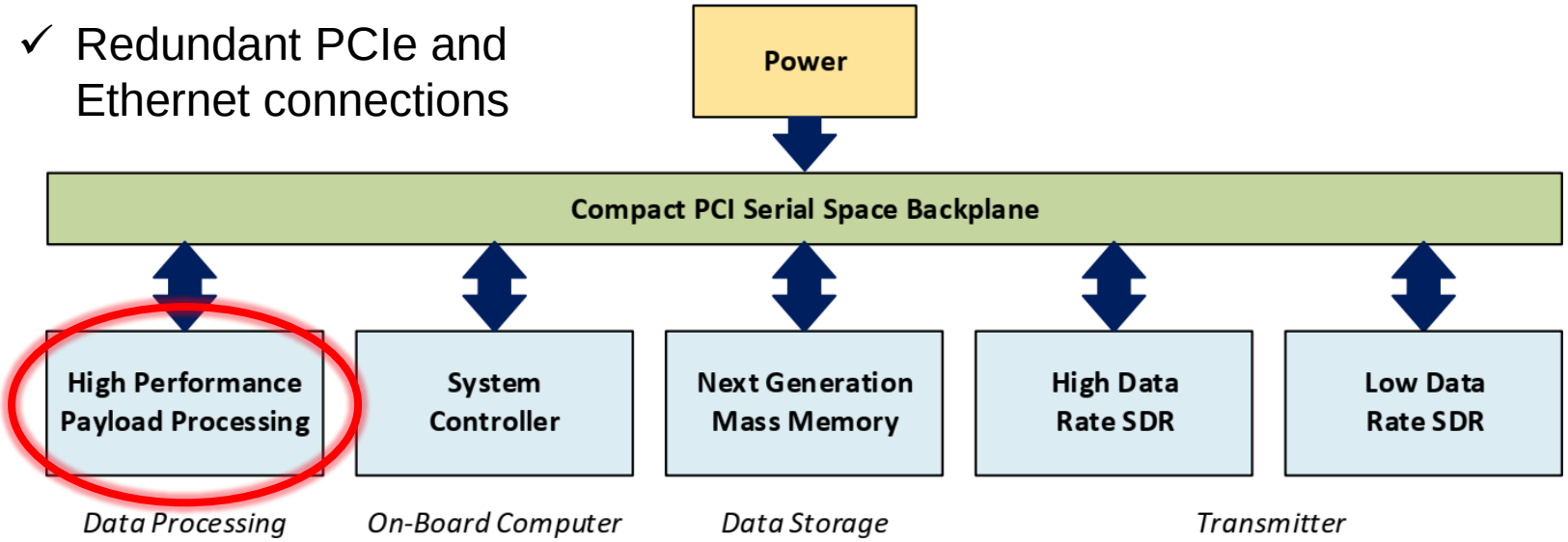
➢ https://www.s4pro-h2020.eu/



cPCI Serial Space Backplane

cPCI-SS standard:

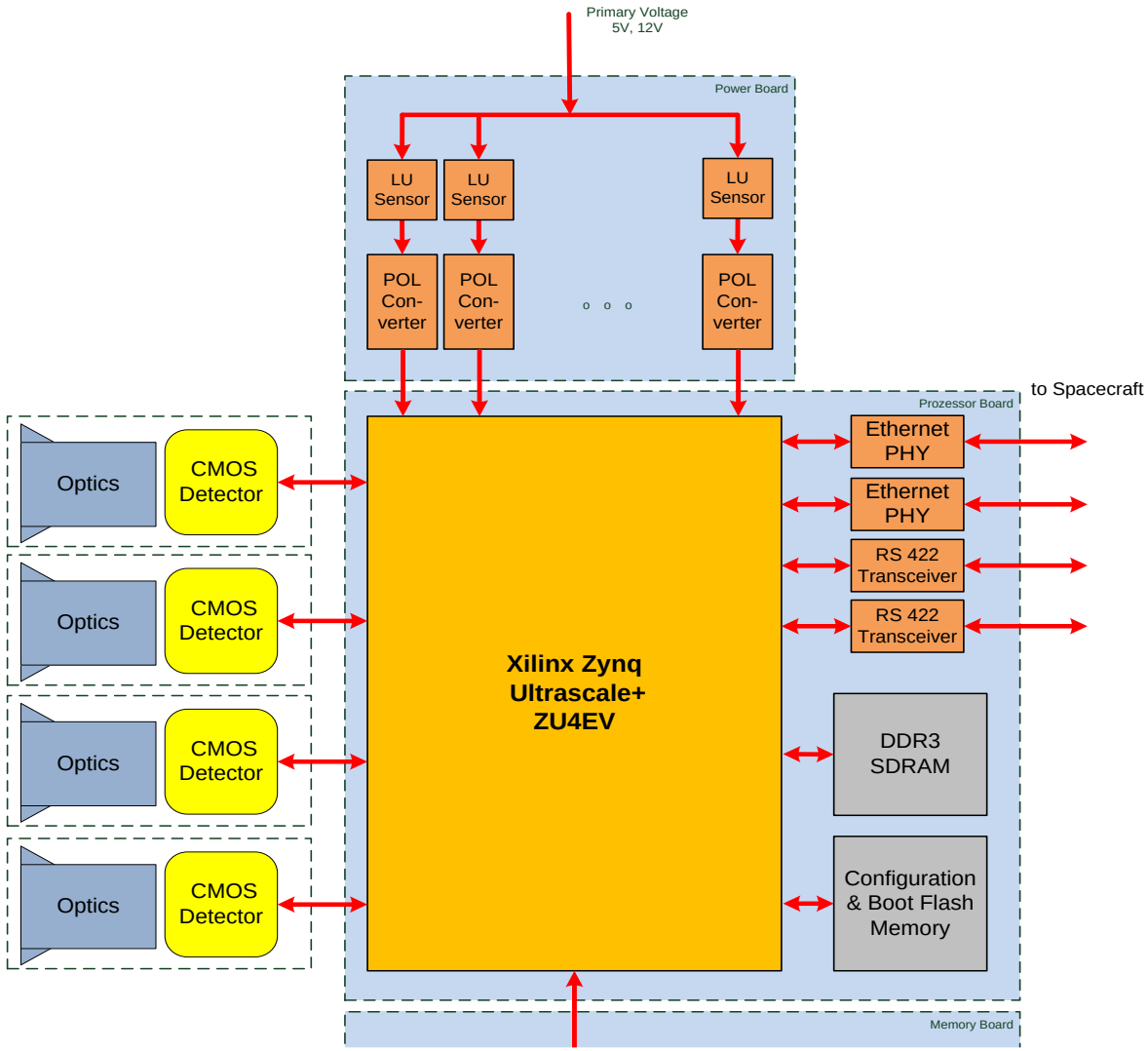
- Flexible solution for payload processing, on-board computing, data storage, and downlink subsystems
- Scalable, able to accommodate different missions with minimal changes
- Multiple hardware vendors
- No single-point-of-failure:
  - ✓ Redundant modules
  - ✓ Redundant PCIe and Ethernet connections



Optional Mass Memory and Video Codec

Xilinx Zynq Ultrascale+ EV-MPSoC including video codec:

- 4 camera command and data IFs
- preprocessing of video
- H.265 compression, 500 Mbit/s per camera
- Expanded by NAND-flash mass memory, 256 GiByte user capacity



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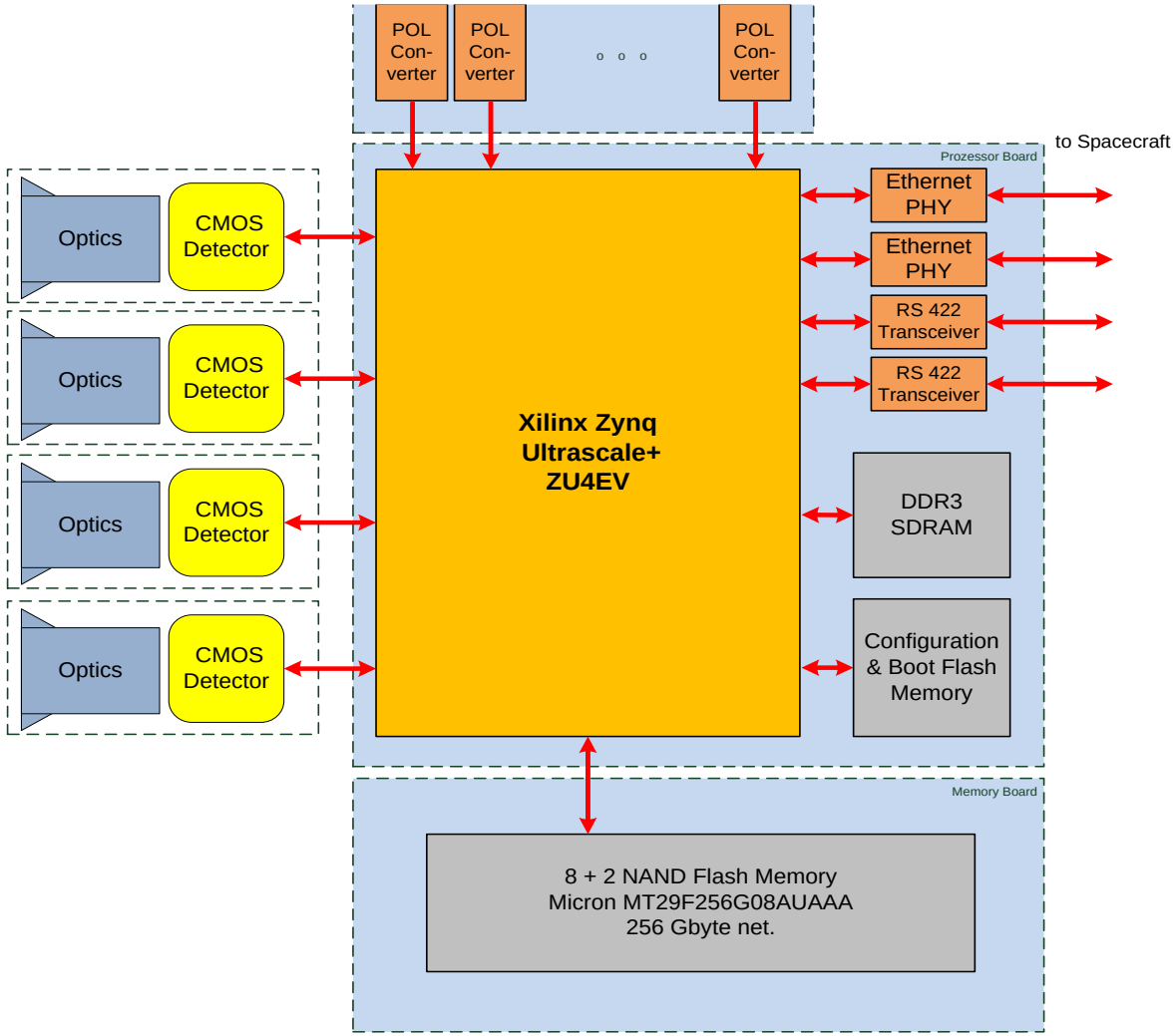
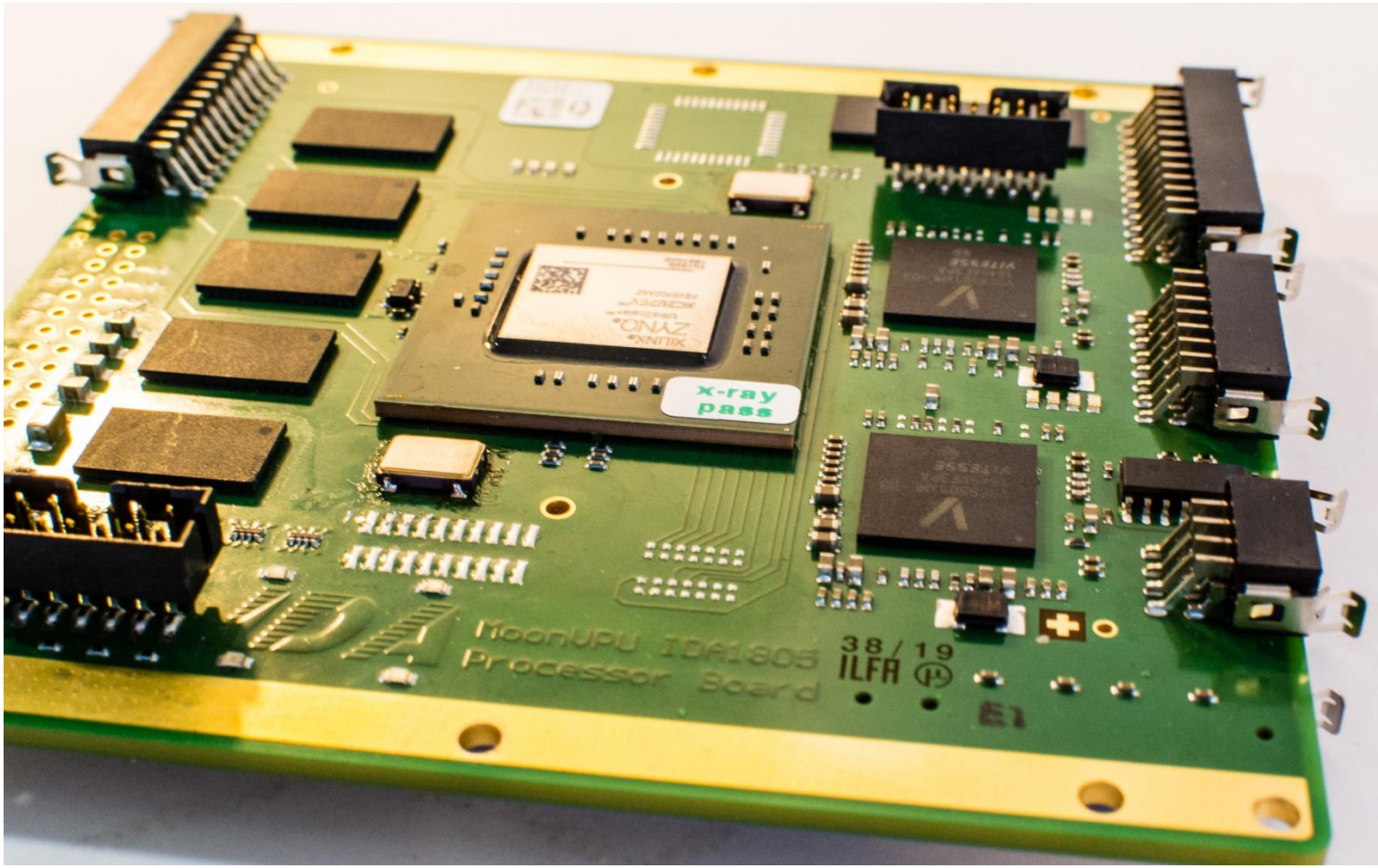


Video Coding Board

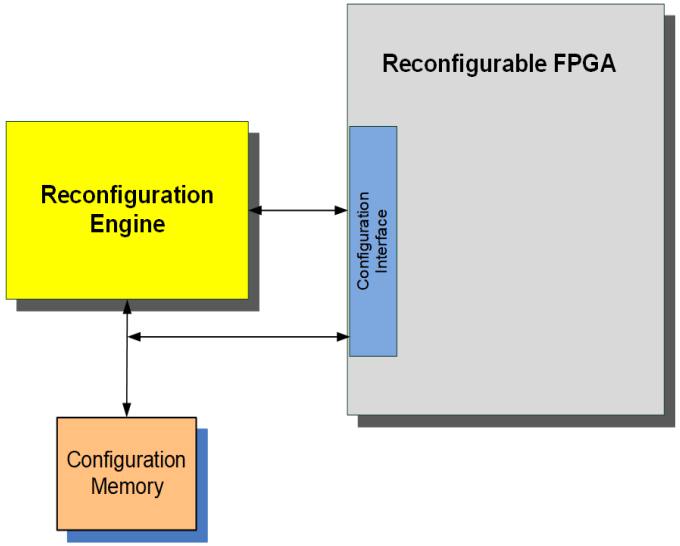


Rad-Hard Version

- Based on Xilinx XQRKU060 Space-grade FPGA
- Additional system controller connector:
  - External rad-hard engine for different types of reconfiguration and scrubbing
  - Fault injection (FDIR)
- Complete Reed-Solomon RS (12, 8) EDAC for external memory
- 3D-Plus QSPI TMR NOR-Flash
- Rad-hard Intersil POL power regulators

➢ *One option in pre-development study for the Lagrange PMI instrument DPU as follow-on of SO/PHI.*

➢ *ESA study: Strategies for reliable on-board reconfiguration of FPGAs*



Conclusion

High performance on-board payload processing in S4Pro:

- Flexible processing module using state-of-the-art reconfigurable FPGAs
- Xilinx Zynq Ultrascale+ MPSoC device
  - ➢ tightly coupled processor-FPGA SoC
- cPCI Serial Space standard
- Throughput of tens of Gbit/s
- Improved Reliability against SEEs
- DDR3 Memory Error Correction
- Single 3U board

Optional Mass Memory and Video Codec, Zynq Ultrascale+ EV-MPSoC

Version based on Xilinx XQRKU060 Space-grade FPGA

- ➢ external rad-hard reconfiguration engine