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# Directional Coupler Design Advancements for Non-Deterministic C-NOT Implementation

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## Introduction

Photons are the natural way to distribute information, both in classical and quantum perspectives, due to the low interaction with the environment and photon-photon interaction. **Silicon Photonics (SiPh)**, thanks to the high refractive index, the low spectral dispersion and the **compatibility with CMOS technology**, opens the way for an easy integration of complex optical systems, all working in the telecom C-band, with integrated electronic circuits.

**Quantum circuits based on SiPh** have been used to implement and test several quantum optical circuits, from silica-on-silicon of relatively few gate systems, to very large multidimensional quantum entanglement circuits. The simplest and universal quantum gate is the **two qubit Controlled-NOT gate (C-NOT)**. The first photonic circuit to be fully developed, produced and tested within our project is constituted by this quantum gate.

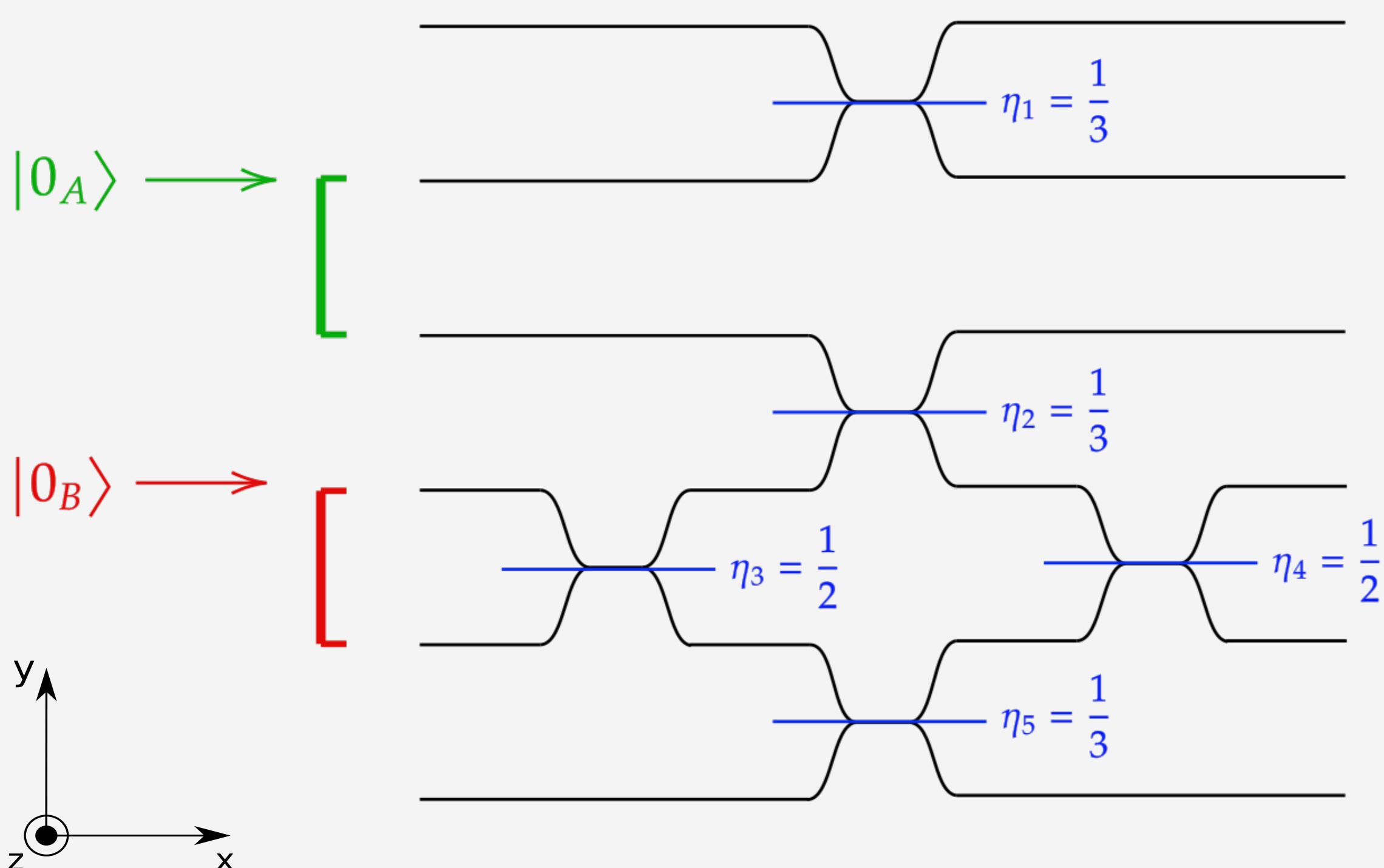
Main constituent device of the C-NOT gate is represented by the **Directional Coupler (DC)**: **this poster describes the simulations and the design of the first SiPh circuit submission of the QUANTEP** which will allow full characterization of the optical, physical and sizing properties of the DCs. The test of this SiPh chip will permit to lay the foundations for the C-NOT gate design and for more complex SiPh circuits.

## C-NOT Gate

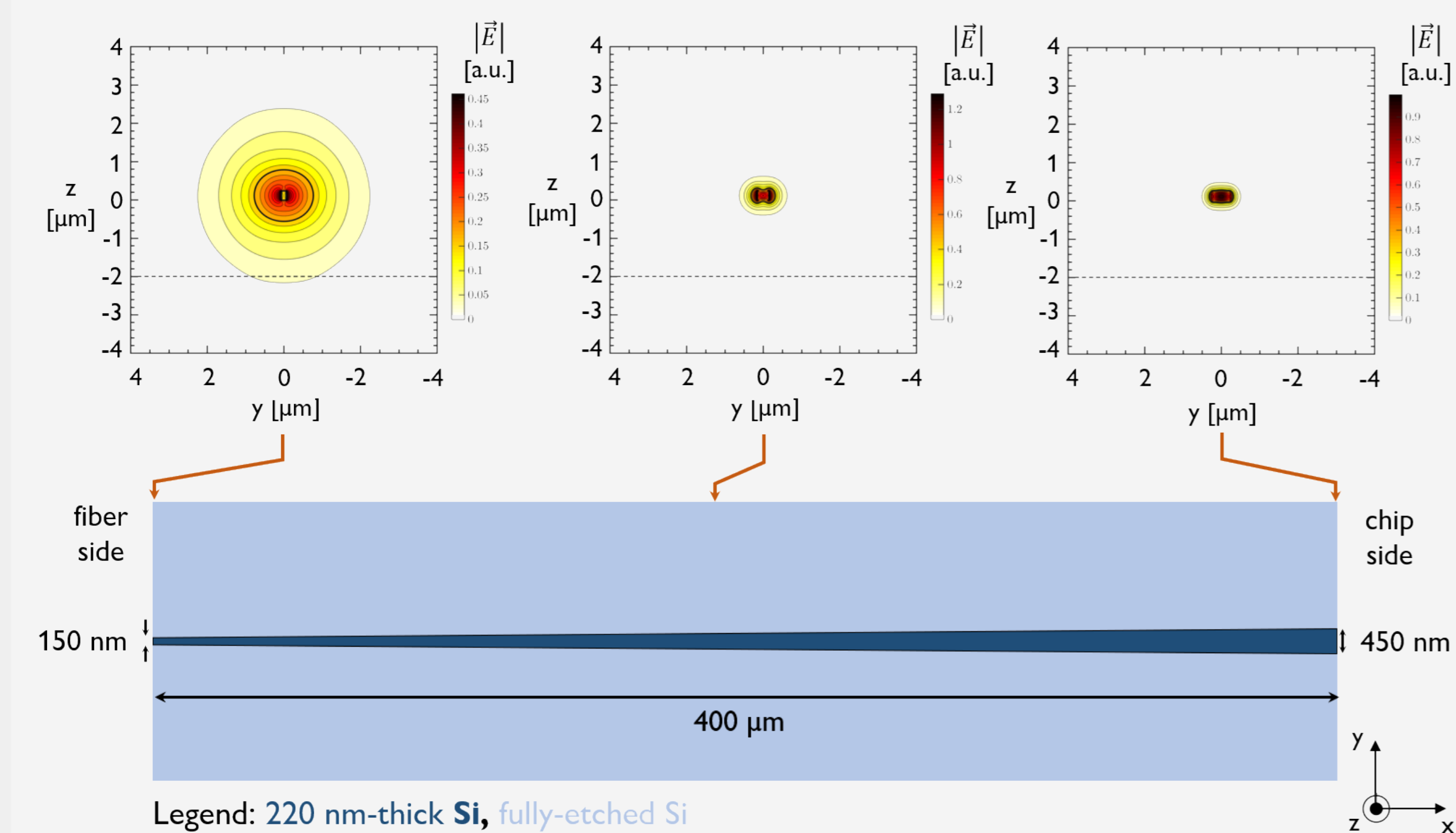
The configuration we have chosen follows T.C. Ralph's paper scheme [1], which makes use of a **linear coincidence basis gate that performs all the operations of a controlled, non deterministic, C-NOT gate** and requires only **single photons** at the input.

Two photonic qubits A and B are encoded in pairs of waveguides in a so-called **dual rail logic**.

The C-NOT gate is composed by 5 DCs which need to be designed in order to achieve **two different Transmission Splitting Ratios at their arms**: ( $T = 1=2; R = 1=2$ ) and ( $T = 2=3; R = 1=3$ ).



## On-chip Silicon Inverse-Taper Spot-Size Converters

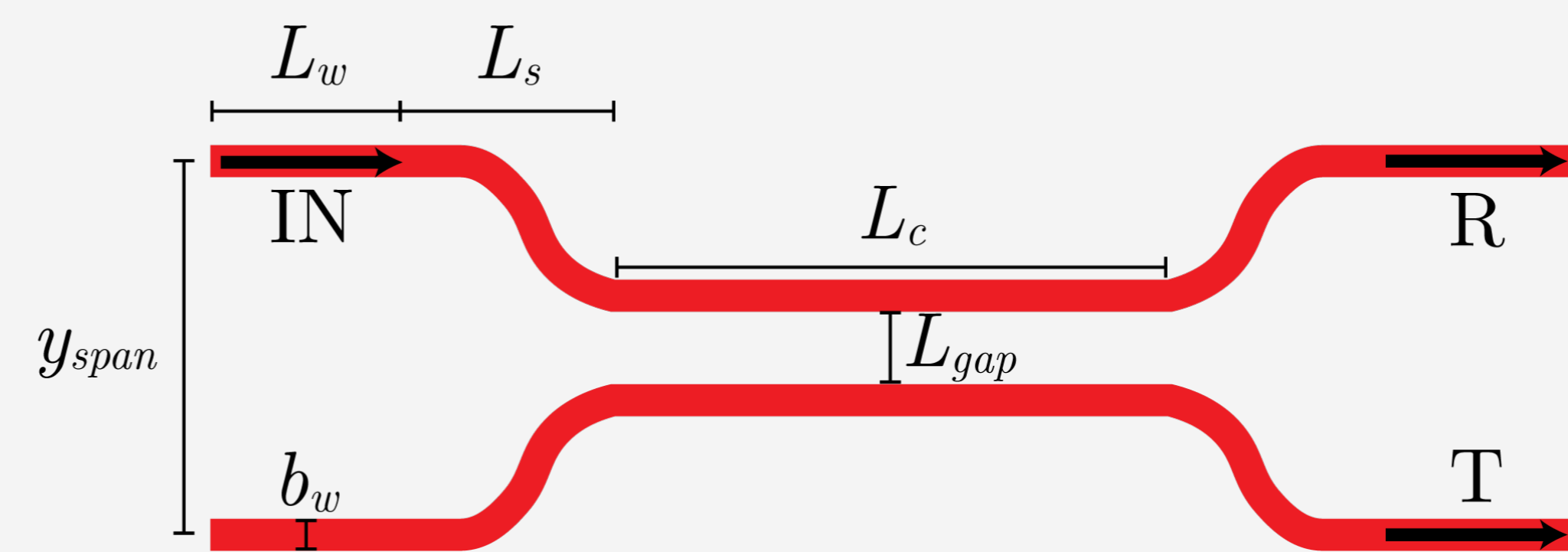


**Fiber edge coupling** have been selected as fiber interfacing strategy to **avoid mode/polarization spurious conversions**.  
**On-chip spot size converters** have been implemented to (partially) **address the mode size mismatch** between silicon waveguides and single-mode optical fibers, relaxing alignment accuracy requirements.  
**Silicon inverse taper design** has been chosen to enlarge the guided optical mode.

[1] T. C. Ralph, N. K. Langford, T. B. Bell, and A. G. White, "Linear optical controlled-NOT gate in the coincidence basis," *Phys. Rev. A*, vol. 65, p. 062324, Jun 2002.  
 [2] A. Yariv, *Quantum Electronics*. John Wiley & Sons, Inc., 1989, ch. 22.

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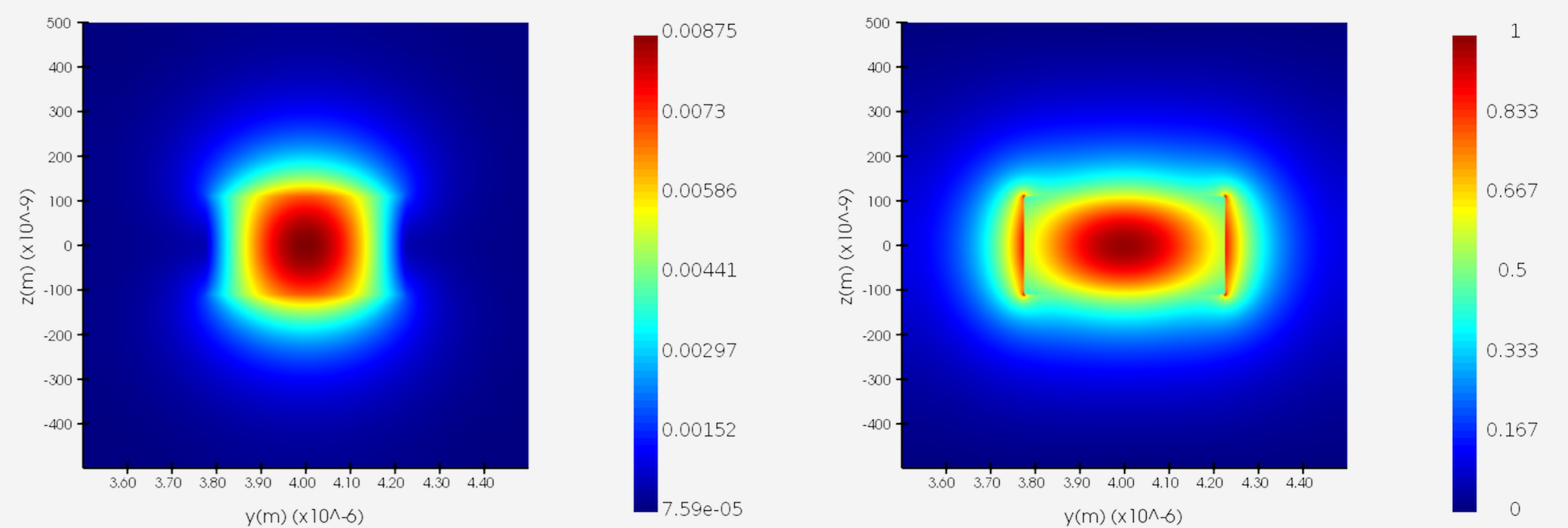
## Directional Coupler



The DC will be integrated in the SiPh circuit and made with **Si waveguides surrounded by SiO<sub>2</sub> cladding**. Dimensions of each waveguide is 0.45 μm width ( $b_w$ ) and 0.22 μm height.  
 In order to achieve the correct splitting ratios we have taken as reference the Transfer Equation elaborated from Yariv [2]. In particular, to get the desired value we have leveraged on the **variation of  $L_{gap}$  and  $L_c$**  which are the most characterizing geometrical parameters:

$$T(L_{gap}; L_c) = \sin^2 \left[ \frac{\pi}{2} \frac{n_{Si}^2 n_{SiO_2}^2 e^{i k_0 L_{gap}}}{n_{eff} b_w + \frac{2}{k_0} \frac{n_{Si}^2 n_{SiO_2}^2}{n_{eff}^2}} \right]$$

**Fundamental Mode** ( $k_0 = 2\pi/\lambda_0$ ,  $\lambda_0 = 1.550 \mu m$  and mode effective refraction index  $n_{eff}$ ) has been chosen for our simulation. Figures show  $H$  field distribution (left) and  $E$  field distribution (right).



## Simulation Results

We have simulated three values of  $L_{gap}$ : 0.25 μm, 0.3 μm, and 0.4 μm.  
 From the simulation data fit, for each  $L_{gap}$  configuration we calculated the optimal  $L_c$  for achieving the desired splitting ratios (Fig. c):  
 $T = 1=2; R = 1=2$  (Fig. a)  
 $T = 2=3; R = 1=3$  (Fig. b)

## Conclusions and Future Developments

The characterization of the **DC configurations will be implemented in a first batch SiPh chip** produced by Tyndall Institute (example figure below) and will undergo **lithographic tuning** on  $L_{gap}$  parameter  
 After production, relevant optical properties will be assessed through optical fiber connection of the chip to the source and to the detectors via the spot size converters.  
 The device floorplan will enable **testing of single-photon Hong-Ou-Mandel interference** with the implemented devices.  
 The same approach described here will be followed for the **realization of the complete C-NOT gate SiPh chip**.