**Scaling Down Channel Dimensions in Thin-Film Transistors: Challenges and Prospects**

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Scaling down channel dimensions of thin-film transistors to submicron and nanoscale dimensions presents several challenges. Successful scaling will enable vastly improved device performance and hence the prospects are certainly very enticing. This presentation presents results and discussion of scaling issues in organic/polymer, amorphous metal oxide, and printed single walled carbon nanotube thin-film transistors (TFTs). One of the biggest challenges is in making suitably good doped source and drain regions to facilitate relatively low-resistance contacts. A more thorough understanding of velocity saturation mechanisms and charge transport at high electric fields is also necessary. We describe charge transport in oxide and polymer TFTs with an emphasis on scaling. We show that for some TFTs, scaling of the channel width facilitates scaling down of channel length and a nanostripe or nanogroove array channel geometry has advantages. Finally, we describe hybrid TFTs – with multiple materials that are better suited to scaling down. The future prospects of scaled down TFTs are discussed.