**Scalable nanomechanical computing**

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**Introduction**

Semiconductor computer architectures, while ubiquitous, face significant challenges in maintaining Moore’s Law in their miniaturisation; in energy consumption, still constrained many orders of magnitude above the Neumann-Landauer information erasure limit; and in operation in radiation harsh environments such as earth-orbit or deep-space. Computers built from nanomechanical components have been proposed as a potential long-term solution to all of these challenges [1]. However, to date, no scalable nanomechanical computing architecture has been demonstrated. The most successful architectures have been based on a hybrid approach where after each operation the outcomes nanomechanical gates are electrically read-out, typically with efficiency beneath one part in a million, and fed-forward onto downstream gates [2].

**Aims, methods and results**

In this talk I will report a new approach to nanomechanical logic circuitry, transferring techniques from photonics to phononics (the study of the flow of mechanical vibrations on a chip). The circuit consists of phononic waveguides or “wires” we have developed (see Fig. 1), that cascade between nonlinear nanomechanical elements, removing the need for electrical interconnects. All logical processes can be achieved in phononics, with electrical readout only of the final computer outcomes. The key components of the computing architecture are single mode phononic waveguides record low attenuation of 1 dB/cm [3], and mechanical resonators with dissipation engineered to minimise losses of mechanical energy within the circuit and quality factors exceeding a million [4]. I will report the demonstration of a universal set of nanomechanical logic gates.

Figure 1a&b show a typical phononic chip contained in a test chamber. Fig. 1c shows the dispersion relations for acoustic modes propagating down a phononic waveguide consisting of a narrow highly stressed silicon nitride film, showing the zero-, single- and multi-mode frequency regimes. Fig. 1d shows experimental results imaging the acoustic mode and confirming single mode operation [3].

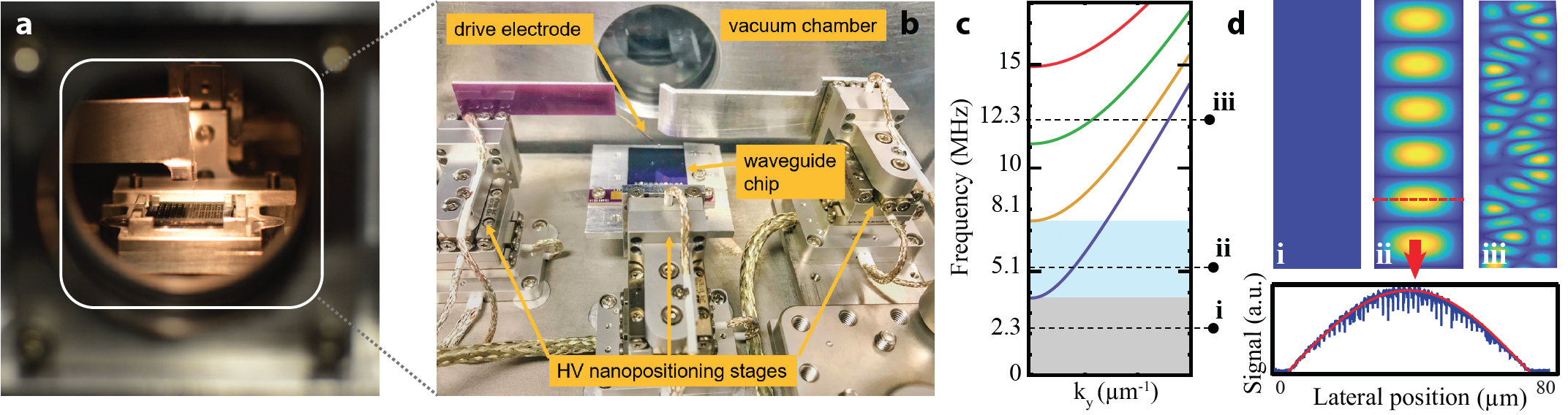


Figure 1: (a) Phononic chip in sample chamber. (b) Inside view describing the main elements. (c) Calculated dispersion relation of phononic waveguide. (d) Top: mode profiles below the waveguide bandgap (i), in the single mode frequency window (ii) and in the multimode window (iii). Bottom: Experimental profile in the single mode window. Red lines: theory.

**References**

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