## Modeling Gate Leakage Current of 0.5 µm GaN HEMTs Operating at 500 °C for RF Applications

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AlGaN/GaN HEMTs have been shown to be a good candidate for high-temperature electronics. Recent reports on hightemperature GaN HEMTs are either with gate lengths above  $1\mu$ m [1], or covers only a limited temperature range [2]. Here we are presenting the gate leakage modeling of 0.5 µm gate length devices designed for RF applications at 500 °C. The gate leakage mechanisms discussed herein are critical to obtain high device reliability and low noise figures at high temperatures.

The GaN HEMTs used in this study were fabricated in NRC's GaN500 process modified for high temperature operation. Fig.1 shows the gate I-V characteristics of the two-fingered HEMTs with 40  $\mu$ m gate width (2×40  $\mu$ m) and 0.5  $\mu$ m gate length. In forward bias, the gate current is dominated by thermal emission up to 2 V. In reverse bias below -1.5 V, the

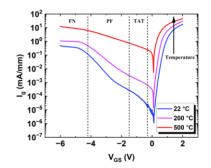


Fig.1. Gate current  $I_g$  vs  $V_{GS}$  of 0.5  $\mu$ m gate-length GaN HEMTs in linear regime ( $V_{DS} = 0.25$  V) at 22, 200, and 500 °C.

trap-assisted tunneling (TAT) model is applied in Fig.2 (a). From -1.5 V to -4.2 V, Poole-Frenkel (PF) emission is found to be dominant. Note that a low-field and high-field region, distinguished by two linear fits in Fig.2 (b), are observed in PF emission at 22 °C and 200 °C. At 500 °C, the slopes of these two regions are approaching the same value. For  $V_{GS} < -4.2$  V, as shown in Fig.2 (c), Fowler Nordheim (FN) tunneling is dominant due to the high electrical field. The parameters in the models above will be presented, interpreted, and discussed.

In summary, we have investigated the gate leakage mechanisms of NRC's GaN HEMTs with measured  $f_T$  of 5.3 GHz at 500 °C (V<sub>GS</sub> = -3 V, V<sub>DS</sub> = 15 V). Modeling shows that PF emission dominates the gate to source leakage current at the gate bias showing peak  $f_T$  with limited drain effect. Further process optimization to minimize PF emission will help to reduce the gate leakage to enable better device performance at 500 °C.

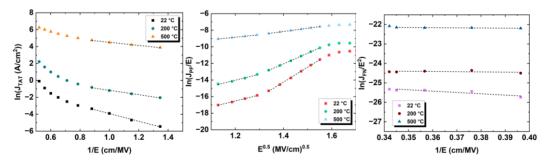


Fig.2. (a)  $In(J_{TAT})$  vs 1/E at 22 °C, 200 °C and 500 °C with linear fits showing trap-assisted tunneling effect. (b)Temperaturedependent  $In(J_{PF}/E)$ as a function of  $\sqrt{E}$  showing low-field and high-field Poole-Frenkel emission. (c) Fowler-Nordheim tunneling plot  $In(J_{FN}/E^2)$  vs 1/E at 22 °C, 200 °C and 500 °C.

References

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