

Hole Spin Qubits in Planar Silicon CMOS

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Spin qubits in silicon and germanium quantum dots are attracting significant interest as building blocks for scalable quantum processors. Semiconductor holes possess a strong intrinsic spin-orbit interaction which enables fast all-electrical spin control via electric-dipole spin resonance (EDSR) using local gate electrodes to both confine and control the hole spins [1]. They also offer rich spin physics, due to spin-3/2 nature of holes and the interplay between quantum confinement, non-uniform strain fields, spin-orbit interaction, and external magnetic fields – and hole spin qubits enable this spin physics to be probed with exquisite resolution.

Here I present results on hole spin qubits fabricated in industry standard planar silicon MOS structures [2,3], using electrostatic gates to define the quantum dots and control the inter-dot tunnel coupling. These devices can be operated in two modes: (i) using two holes in adjacent quantum dots we define a single ‘singlet-triplet’ qubit and have demonstrated coherent operations with T1 times of 10 μ s, singlet-triplet oscillation frequencies up to 400 MHz, and coherence times up to 600 ns (enhanced to 1.3 μ s with refocusing techniques) [4]. (ii) We can also use the same architecture to operate a two qubit system where we manipulate the individual spin states in each dot with microwave pulses applied to the gate electrodes. For these ‘spin-orbit’ qubits we demonstrate Rabi frequencies reaching 15 MHz and controllable two-qubit exchange at \sim 40 MHz.

Importantly many of these results were obtained with devices fabricated on a 300mm wafer compatible with foundry-based fabrication processes [3], affirming industrially fabricated planar MOS silicon quantum dots as a platform for high quality spin qubits.

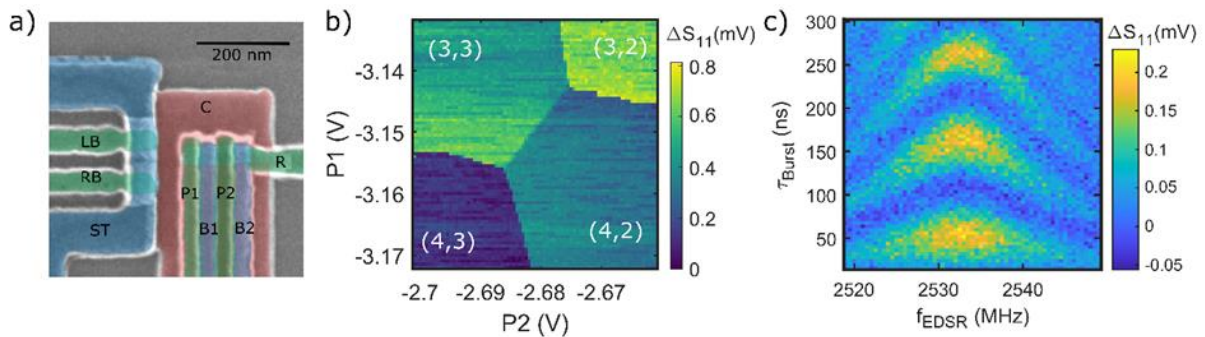


Fig.1. a) False-colour SEM image of the device, where the quantum dots are formed under the plunger gates P1 and P2, with confinement provided by the barrier gates B1, B2 and the C-gate. An adjacent single-hole transistor is used for charge sensing and readout. b) Charge stability diagram in the few-hole, weakly-coupled regime where spin readout is performed. c) Rabi oscillations as a function of frequency detuning showing a typical chevron pattern.

References

- [1] R. Maurand *et al.* Nat Commun. 7, 13575 (2016); H. Watzinger *et al.* Nature Commun. 9, 3902 (2018); N.W. Hendrickx *et al.* Nature 577, 487 (2020); F.N.M. Froning *et al.* Nat. Nanotechnol. 16, 308 (2021).
- [2] Ik Kyeong Jin *et al.* Nano Letters 23, 1261 (2023); S.D. Liles *et al.* Nature Commun. 9, 3255 (2018).
- [3] R. Li *et al.*, 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2020, pp. 38.3.1-38.3.4, doi: 10.1109/IEDM13553.2020.9371956; N. I. D. Stuyck *et al.*, 2021 Symposium on VLSI Circuits, Kyoto, Japan, 2021, pp. 1-2, doi: 10.23919/VLSICircuits52068.2021.9492427.
- [4] S.D. Liles *et al.*, arXiv:2310.09722 (2023).