Si quantum dot qubits interfaced with monolithic ultra-low power Cryo-CMOS

J. Lehtinen, N. Yurttagül, M. Kainlauri, J. Toivonen, S. Khadka, and M. Prunnila
SemiQon Technologies, Tietotie 3, 02150 Espoo
janne.lehtinen@semiqon.tech

Complex microsystems typically include interfacing analog and/or digital electronics integrated into the microsystem by heterogenous or monolithic methods. In many applications the interfacing is handled by silicon-based CMOS circuits. MOSFETs naturally function also at low temperatures and, therefore, if properly designed, Si CMOS circuits build from these can operate at cryogenic temperatures even down to sub-Kelvin range. Low temperature CMOS, so-called cryo-CMOS, has been investigated and utilized widely for various cryo-enabled applications. Recently, the rise of quantum technologies has increased the demand of high performance cryo-electronics, especially, for interfacing solid-state quantum processors and the field has turned its attention towards cryo-CMOS [1,2].

In this communication, we report on Si quantum dot (QD) arrays interfaced with monolithic CMOS circuitry (Fig. 1). We use our in-house FDSOI technology (~20 nm-thick Si channel) to fabricate the QD and CMOS on the same wafer. The QDs are defined by Si mesa geometry and two layers of gates. The fabrication/technology is similar to the one reported by some of the authors in Ref. [3].

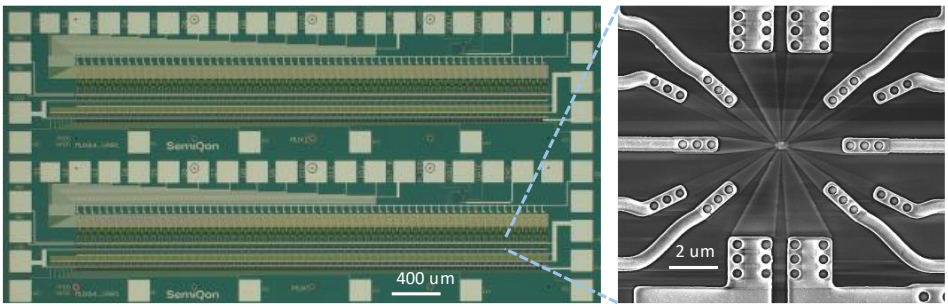

Fig. 1. Left: Microscope image of QD-CMOS chip. Right: SEM image of a QD device.

The challenge in using Si CMOS circuits at low temperatures is their power dissipation, which is determined by the FET switching characteristics. Channel disorder broadens the density of states at low carrier densities close to the threshold and, therefore, CMOS transistor switching does not sharpen down to the lowest temperatures, but typically exhibits a freezeout at temperature $T = T_{FO}$. This inherently leads to non-optimal speed and energy consumption below T_{FO}. Modern gate stack of CMOS has HfO gate oxide, which introduces relatively strong disorder, and such transistors typically have T_{FO} above 30 K [4]. Classical SiO2 gate dielectric provides less disorder resulting smaller T_{FO} down to ~15 K [3].

Our CMOS transistors show ultra-sharp switching characteristics at cryogenic temperatures indicating T_{FO} even in sub-kelvin range. We will discuss the physical mechanisms behind the sharp switching - intimately coupled to the nature of the disorder in the transistor channel. The low T_{FO} enables, for example, low power operation of CMOS, which, thereby, can be integrated in close vicinity with sensitive quantum devices like QD spin qubits. We will present properties of hybrid CMOS – QD cryo-microsystems, where the QDs are interfaced with ultra-low power cryo-CMOS integrated monolithically on the same chip.

References

[1] B. Patra *et al*., IEEE J. of Solid-State Circ. **53**, 309 (2018). https://doi.org/10.1109/JSSC.2017.2737549
[2] X. Xue *et al.* Nature **593**, 205 (2021). https://doi.org/10.1038/s41586-021-03469-4
[3] H. Bohuslavskyi *et al.* https://arxiv.org/abs/2208.12131
[4] H. Bohuslavskyi *et al.* IEEE Electron Dev. Lett. **40**, 784 (2019). https://doi.org/10.1109/LED.2019.2903111