A 2D Semiconductor Route to Spin-valley Qubits

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Van der Waals semiconductors such as 2D transition metal dichalcogenides (TMDs) are attractive for ultra-scaled and low power devices, and exploiting the novel spin-valley coupling for valleytronics [1] and quantum information processing [2, 3]. While exfoliated TMDs are expedient for quick proof-of-concept devices, the scalability for practical applications is still hindered by the lack of complete scalable processing of such materials into devices. Various traditional processes suitable for bulk semiconductors may not lend themselves directly to the fabrication of high-quality TMD devices. From electrical contacts to dielectrics for gating, the layered TMD of atomic thickness requires a near radical rethink of what are well-established rules of thumb for processing bulk semiconductors. In this talk, I'll present our efforts towards establishing scalable fabrication of spin-valley qubits in 2D TMDs. Defects inherent and induced in the TMDs can impair their performance and hence a scientific understanding of how to handle the material defects such or vacancies, unintentional dopants, grain boundaries, and imperfect interfacing with contact or dielectric materials will be critical. I will cover our work towards limiting the impact of oxidation of TMDs, optimizing electrical contacts and dielectric interfaces related to the fabrication of TMD devices [4 – 6]. With such efforts, we have recently achieved gate-defined quantum dot devices [6].

References

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